DECchip 21142 PCI Fast Ethernet LAN Controller

Data Sheet

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1 DECchip 21142 Overview

The DECchip 21142 PCI Fast Ethernet LAN Controller (21142) supports the peripheral component interconnect (PCI) bus. It provides a direct interface connection to the PCI and adapts easily to most other standard buses. The 21142 software interface and data structures are optimized to minimize the host CPU load and to allow for maximum flexibility in the buffer descriptor management. The 21142 contains large onchip FIFOs, so no additional onboard memory is required. The 21142 provides an upgradable boot ROM interface and a CardBus interface connection.

1.1 General Description

The 21142 interfaces with the PCI bus by using onchip control and status registers (CSRs), and a shared CPU memory area that is set up mainly during initialization. This minimizes the processor involvement in the 21142 operation during normal reception and transmission. The 21142 is compliant with the *PCI Local Bus Specification, Revision 2.0 and Revision 2.1*. Bus traffic is also minimized by filtering out received runt frames and by automatically retransmitting collided frames without needing to repeat a fetch from shared memory.

On the network side, the 21142 provides three ports: a 10BASE-T 10Mb/s port, an attachment unit interface (AUI) 10Mb/s port, and a media-independent interface (MII) 100/10Mb/s port. The 10BASE-T port provides a direct Ethernet connection to the twisted-pair (TP) interface. The AUI port provides a direct Ethernet connection to the AUI. The MII port supports a full implementation of the MII standard. The 21142 is also capable of functioning in a full-duplex environment for the three ports.

1.2 Features

The 21142 has the following features:

- Offers a single-chip Fast Ethernet controller for PCI local bus:
  - Provides a direct interface to PCI bus
  - Supports three network ports: 10BASE-T (10Mb/s), AUI (10Mb/s), and MII (10/100Mb/s)
- Provides standard 10/100Mb/s MII supporting CAT3 unshielded twisted-pair (UTP), CAT5 UTP, shielded twisted-pair (STP) and fiber cables
- Enables automatic detection and correction of 10BASE-T receive polarity
- Supports autodetection between 10BASE-T, AUI, and MII ports
- Supports full-duplex operation on both 10Mb/s and 10/100Mb/s ports
- Provides external and internal loopback capability on both ports
- Contains a variety of flexible address filtering modes (including perfect, hash tables, inverse perfect, and promiscuous):
  - 16 perfect addresses (normal or inverse filtering)
  - 512 hash-filtered addresses
  - 512 hash-filtered multicast addresses and one perfect address
  - Pass all multicast
  - Promiscuous
  - Pass all incoming packets with a status report
- Offers a unique, patented solution to Ethernet capture-effect problem
- Contains large independent receive and transmit FIFOs; no additional onboard memory required
- Includes a powerful onchip direct memory access (DMA) with programmable burst size, providing for low CPU utilization
- Implements unique, patent-pending intelligent arbitration between DMA channels to minimize underflow or overflow
- Supports PCI clock frequency from dc to 33 MHz; network operational with PCI clock from 25 MHz to 33 MHz
- Supports an unlimited PCI burst
- Supports PCI read multiple command

- Supports early interrupt on transmit
- Implements low power management with two power saving modes (sleep or snooze)
- Supports both PCI 5.0-V and 3.3-V signaling environments
- Supports either big or little endian byte ordering for buffers and descriptors
- Contains 4-bit, general-purpose, programmable register and corresponding I/O pins
- Supports interrupts from two general-purpose pins
- Provides LED support for various network activity indications
- Provides MicroWire interface for serial ROM (1K and 4K EEPROM)
- Provides an upgradable boot ROM (flash or EEPROM) interface of up to 256KB
- Supports automatic loading of subvendor ID configuration register
- Includes CardBus support
- Implements JTAG-compatible test-access port with boundary-scan pins
- Supports IEEE 802.3 and ANSI 8802-3 standards
- Implements low-power, 3.3-V complementary metal-oxide semiconductor (CMOS) process technology

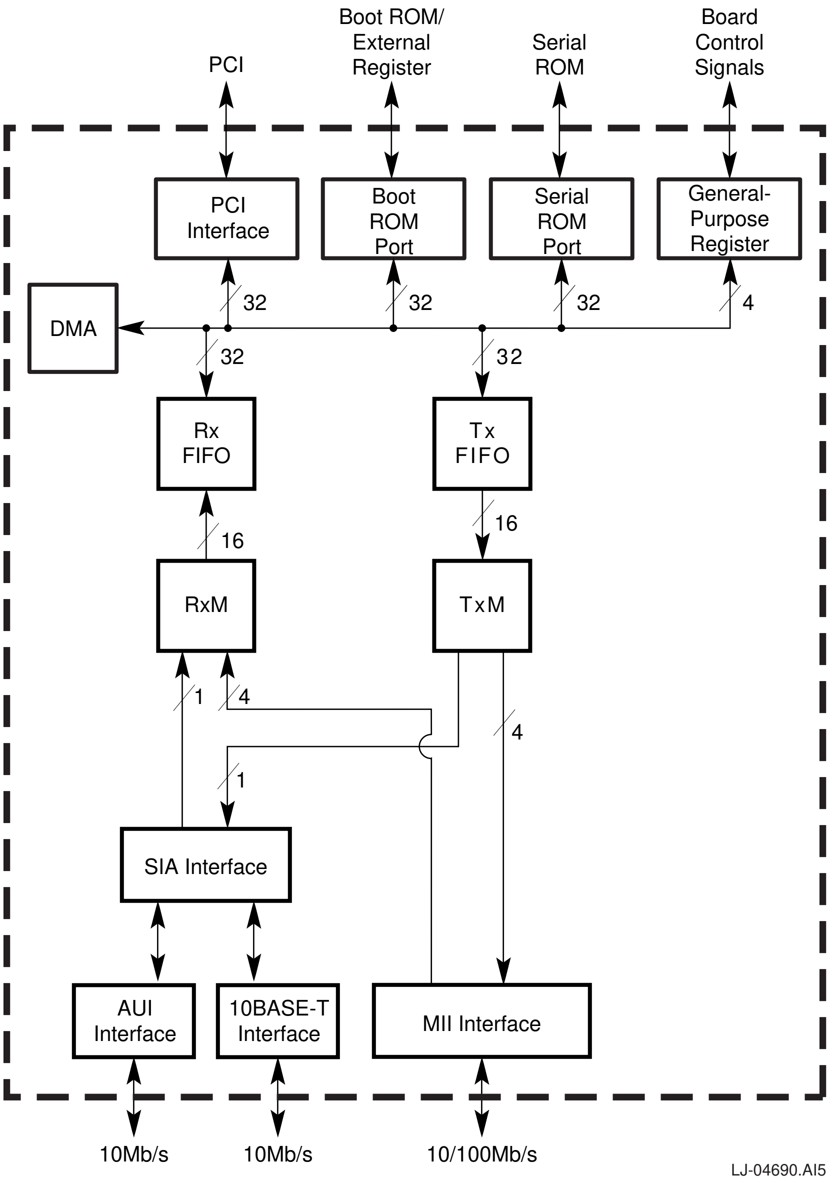
1.3 Microarchitecture

The following list describes the 21142 hardware components, and Figure 1 shows a block diagram of the 21142:

- PCI interface—Includes all interface functions to the PCI bus; handles all interconnect control signals; and executes PCI DMA and I/O transactions
- DMA—Contains dual receive and transmit controller; supports bursts of up to 32 longwords; handles data transfers between CPU memory and onchip memory
- FIFOs—Contains two FIFOs for receive and transmit; supports automatic packet deletion on receive (runt packets or after a collision) and packet retransmission after a collision on transmit
- TxM—Handles all CSMA/CD[1] MAC[2] transmit operations, and transfers data from transmit FIFO to the ENDEC for transmission
- RxM—Handles all CSMA/CD receive operations, and transfers the data from the ENDEC to the receive FIFO
- SIA interface—Performs physical layer operations; implements the AUI and 10BASE-T functions, including the Manchester encoder and decoder functions
- General-purpose register—Enables software use for input or output functions and LED indications
- MII interface—Provides a full MII signal interface
- Serial ROM port—Provides a direct interface to the MicroWire Ethernet address ROM and system parameters
- Boot ROM port—Includes the required interface to the boot ROM for read and write operations; supports accesses to bytes or longwords (32-bit) and provides the ability to connect an external 8-bit register to the boot ROM port

[1] Carrier-sense multiple access with collision detection
[2] Media access control

Figure 1 DECchip 21142 Block Diagram



2 Pinout

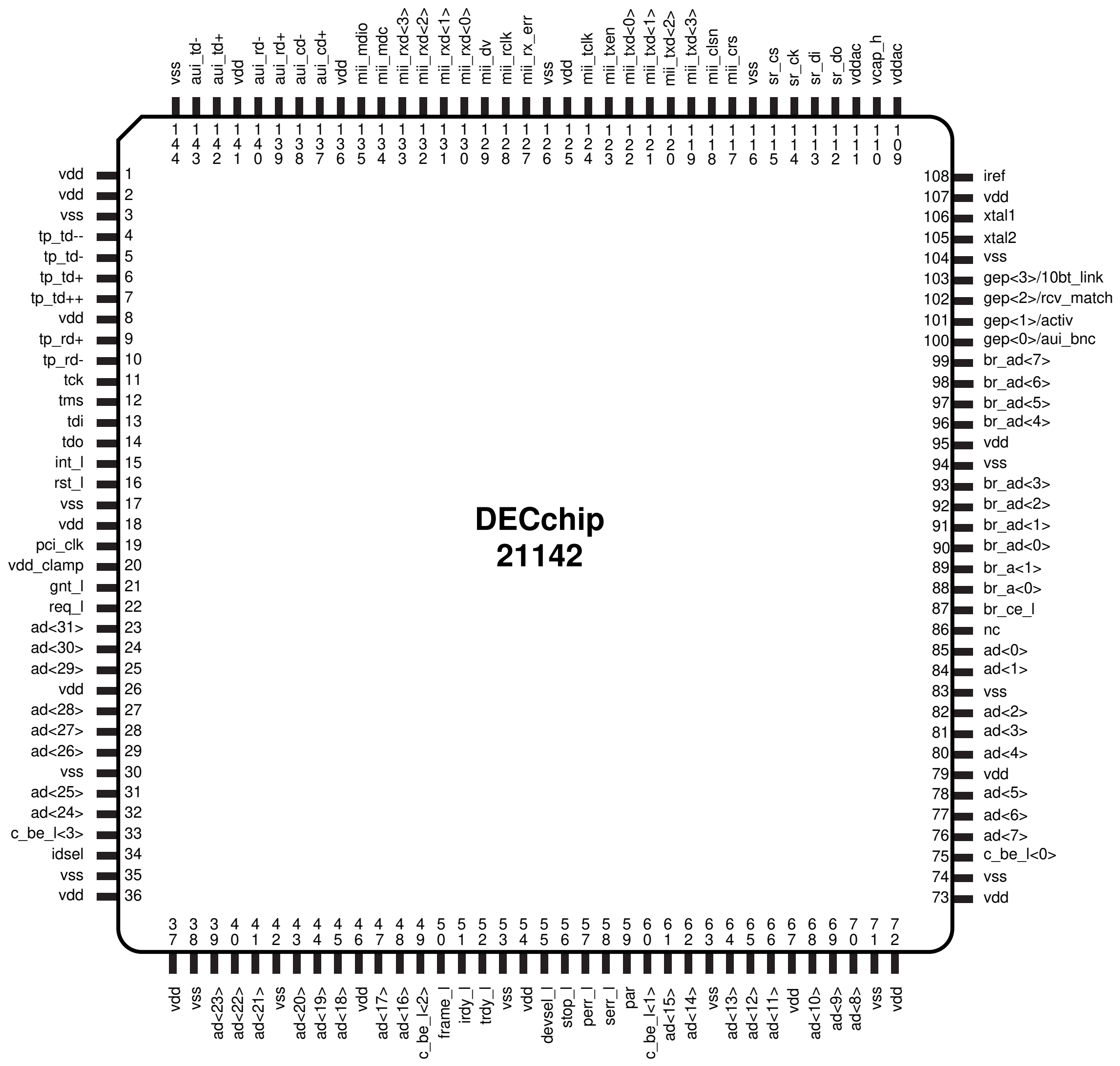
The 21142 is packaged in a 144-pin plastic quad flat pack (PQFP). The tables in this section provide a description of the pins and their respective signal definitions.

Table 1 lists the tables in this section. Figure 2 shows the 21142 pinout.

Table 1 Index to Pinout Tables

For this information . . .	Refer to . . .
Logic signals	Table 2
Power pins	Table 3
Functional signals description	Table 4
Input pins	Table 5
Output pins	Table 6
Input/output pins	Table 7
Open drain pins	Table 8
Signal functions	Table 9

Figure 2 DECchip 21142 Pinout Diagram (Top View)



2.1 Signal Reference Tables

Table 2 provides an alphabetical list of the 21142 logic names and their pin numbers. Table 3 provides a list of the 21142 power pin numbers.

Table 2 Logic Signals

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
ad<0>	85	**ad<24>**	32	**br_ce_l**	87
ad<1>	84	**ad<25>**	31	**c_be_l<0>**	75
ad<2>	82	**ad<26>**	29	**c_be_l<1>**	60
ad<3>	81	**ad<27>**	28	**c_be_l<2>**	49
ad<4>	80	**ad<28>**	27	**c_be_l<3>**	33
ad<5>	78	**ad<29>**	25	**devsel_l**	55
ad<6>	77	**ad<30>**	24	**frame_l**	50
ad<7>	76	**ad<31>**	23	**gep<0>/aui_bnc**	100
ad<8>	70	**aui_cd–**	138	**gep<1>/activ**	101
ad<9>	69	**aui_cd+**	137	**gep<2>/rcv_match**	102
ad<10>	68	**aui_rd–**	140	**gep<3>/10bt_link**	103
ad<11>	66	**aui_rd+**	139	**gnt_l**	21
ad<12>	65	**aui_td–**	143	**idsel**	34
ad<13>	64	**aui_td+**	142	**int_l**	15
ad<14>	62	**br_a<0>**	88	**irdy_l**	51
ad<15>	61	**br_a<1>**	89	**iref**	108
ad<16>	48	**br_ad<0>**	90	**mii_clsn**	118
ad<17>	47	**br_ad<1>**	91	**mii_crs**	117
ad<18>	45	**br_ad<2>**	92	**mii_dv**	129
ad<19>	44	**br_ad<3>**	93	**mii_mdc**	134
ad<20>	43	**br_ad<4>**	96	**mii_mdio**	135
ad<21>	41	**br_ad<5>**	97	**mii_rclk**	128
ad<22>	40	**br_ad<6>**	98	**mii_rx_err**	127
ad<23>	39	**br_ad<7>**	99	**mii_rxd<0>**	130

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Table 2 (Cont.) Logic Signals

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
mii_rxd<1>	131	**perr_l**	57	**tms**	12
mii_rxd<2>	132	**req_l**	22	**tp_rd–**	10
mii_rxd<3>	133	**rst_l**	16	**tp_rd+**	9
mii_tclk	124	**serr_l**	58	**tp_td–**	5
mii_txd<0>	122	**sr_ck**	114	**tp_td– –**	4
mii_txd<1>	121	**sr_cs**	115	**tp_td+**	6
mii_txd<2>	120	**sr_di**	113	**tp_td+ +**	7
mii_txd<3>	119	**sr_do**	112	**trdy_l**	52
mii_txen	123	**stop_l**	56	**vcap_h**	110
nc	86	**tck**	11	**xtal1**	106
par	59	**tdi**	13	**xtal2**	105
pci_clk	19	**tdo**	14	—	—

Table 3 Power Pins

Signal	Pin Numbers	Signal	Pin Numbers
vdd (3.3 V)	1, 2, 8, 18, 26, 36, 37, 46, 54, 67, 72, 73, 79, 95, 107, 125, 136, 141	**vss** (GND)	3, 17, 30, 35, 38, 42, 53, 63, 71, 74, 83, 94, 104, 116, 126, 144,
vddac (3.3 V)	109, 111		
vdd_clamp (5 V/3.3 V)	20		

Table 4 provides a functional description of each of the 21142 signals. These signals are listed alphabetically. The functional grouping of each pin is listed in Section 2.3.

The following terms describe the 21142 pinout:

- **Address phase**

  Address and appropriate bus commands are driven during this cycle.

- **Data phase**

  Data and the appropriate byte enable codes are driven during this cycle.

- **_l**

  All pin names with the _l suffix are asserted low.

The following abbreviations are used in Table 4:

I = Input
O = Output
I/O = Input/output
O/D = Open drain
P = Power

Table 4 Functional Description of DECchip 21142 Signals

Signal	Type	Pin Number	Description
ad<31:0>	I/O	See Table 2.	32-bit PCI address and data lines. Address and data bits are multiplexed on the same pins. During the first clock cycle of a transaction, the address bits contain a physical address (32 bits). During subsequent clock cycles, these same lines contain 32 bits of data. A 21142 bus transaction consists of an address phase followed by one or more data phases. The 21142 supports both read and write bursts (in master operation only). Little and big endian byte ordering can be used.
aui_cd–	I	138	Attachment unit interface receive collision differential negative data.
aui_cd+	I	137	Attachment unit interface receive collision differential positive data.

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Table 4 (Cont.) Functional Description of DECchip 21142 Signals

Signal	Type	Pin Number	Description
aui_rd–	I	140	Attachment unit interface receive differential negative data.
aui_rd+	I	139	Attachment unit interface receive differential positive data.
aui_td–	O	143	Attachment unit interface transmit differential negative data.
aui_td+	O	142	Attachment unit interface transmit differential positive data.
br_a<0>	O	88	Boot ROM address line bit 0. In a 256KB configuration, this pin also carries in two consecutive address cycles, boot ROM address bits 16 and 17.
br_a<1>	O	89	Boot ROM address line bit 1. This pin also latches the boot ROM address and control lines by the two external latches.
br_ad<7:0>	I/O	See Table 2.	Boot ROM address and data multiplexed lines bits 7 through 0. In two consecutive address cycles, these lines contain the boot ROM address pins 7 through 2, **oe_l** and **we_l** in the first cycle; and these lines contain boot ROM address pins 15 through 8 in the second cycle. During the data cycle, bits 7 through 0 contain data.
br_ce_l	O	87	Boot ROM or external register chip enable.
c_be_l<3:0>	I/O	See Table 2.	Bits 0 through 3 of the bus command and byte enable lines. Bus command and byte enable are multiplexed on the same PCI pins. During the address phase of the transaction, these 4 bits provide the bus command. During the data phase, these 4 bits provide the byte enable. The byte enable determines which byte lines carry valid data. For example, bit 0 applies to byte 0, and bit 3 applies to byte 3.

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Table 4 (Cont.) Functional Description of DECchip 21142 Signals

Signal	Type	Pin Number	Description
devsel_l	I/O	55	Device select is asserted by the target of the current bus access. When the 21142 is the initiator of the current bus access, it expects the target to assert **devsel_l** within 5 bus cycles, confirming the access. If the target does not assert **devsel_l** within the required bus cycles, the 21142 aborts the cycle. To meet the timing requirements, the 21142 asserts this signal in a medium speed (within 2 bus cycles).
frame_l	I/O	50	The **frame_l** signal is driven by the 21142 (bus master) to indicate the beginning and duration of an access. The **frame_l** signal asserts to indicate the beginning of a bus transaction. While **frame_l** is asserted, data transfers continue. The **frame_l** signal deasserts to indicate that the next data phase is the final data phase transaction.
gep<0>/aui_bnc	I/O	100	This general-purpose pin can be used by software as either a status pin or a control pin. It can be configured by software to: • Perform either input or output functions. Can provide an interrupt when it is an input pin. • Provide an AUI (10BASE5) or BNC (10BASE2) select line. When asserted, the 10BASE5 mode is selected. When deasserted, the 10BASE2 mode is selected. When used as an output pin, it is mainly used to enable the external BNC transceiver in 10BASE2 mode.

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Table 4 (Cont.) Functional Description of DECchip 21142 Signals

Signal	Type	Pin Number	Description
gep<1>/activ	I/O	101	This general-purpose pin can be used by software as either a status pin or a control pin. It can be configured by software to: • Perform either input or output functions. Can provide an interrupt when it is an input pin. • Provide an LED that indicates either receive or transmit activity.
gep<2>/rcv_match	I/O	102	This general-purpose pin can be used by software as either a status pin or a control pin. It can be configured by software to: • Perform either input or output functions. • Provide an LED that indicates a receive packet has passed address recognition.
gep<3>/10bt_link	I/O	103	This general-purpose pin can be used by software as either a status pin or a control pin. It can be configured by software to: • Perform either input or output functions. • Provide an LED that indicates that the 10BASE-T link integrity test has completed successfully after the link was down.
gnt_l	I	21	Bus grant asserts to indicate to the 21142 that access to the bus is granted.

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Table 4 (Cont.) Functional Description of DECchip 21142 Signals

Signal	Type	Pin Number	Description
idsel	I	34	Initialization device select asserts to indicate that the host is issuing a configuration cycle to the 21142.
int_l	O/D	15	Interrupt request asserts when one of the appropriate bits of CSR5 sets and causes an interrupt, provided that the corresponding mask bit in CSR7 is not asserted. Interrupt request deasserts by writing a 1 into the appropriate CSR5 bit. If more than one interrupt bit is asserted in CSR5 and the host does not clear all input bits, the 21142 deasserts **int_l** for one cycle to support edge-triggered systems. This pin must be pulled up by an external resistor.
iref	I	108	Current reference input for the analog phase-locked loop logic.
irdy_l	I/O	51	Initiator ready indicates the bus master's ability to complete the current data phase of the transaction. A data phase is completed on any rising edge of the clock when both **irdy_l** and target ready **trdy_l** are asserted. Wait cycles are inserted until both **irdy_l** and **trdy_l** are asserted together. When the 21142 is the bus master, **irdy_l** is asserted during write operations to indicate that valid data is present on the 32-bit **ad** lines. During read operations, the 21142 asserts **irdy_l** to indicate that it is ready to accept data.
mii_clsn	I	118	Collision detect is asserted when detected by an external physical layer protocol (PHY) device.
mii_crs	I	117	Carrier sense is asserted by the PHY when the media is active.

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Table 4 (Cont.) Functional Description of DECchip 21142 Signals

Signal	Type	Pin Number	Description
mii_dv	I	129	Data valid is asserted by an external PHY when receive data is present on the **mii_rxd** lines and is deasserted at the end of the packet. This signal should be synchronized with the **mii_rclk** signal.
mii_mdc	O	134	MII management data clock is sourced by the 21142 to the PHY devices as a timing reference for the transfer of information on the **mii_mdio** signal.
mii_mdio	I/O	135	MII management data input/output transfers control information and status between the PHY and the 21142.
mii_rclk	I	128	Supports either the 25-MHz or 2.5-MHz receive clock. This clock is recovered by the PHY.
mii_rx_err	I	127	Receive error asserts when a data decoding error is detected by an external PHY device. This signal is synchronized to **mii_rclk** and can be asserted for a minimum of one receive clock. When asserted during a packet reception, it sets the cyclic redundancy check (CRC) error bit in the receive descriptor (RDES0).
mii_rxd<3:0>	I	See Table 2.	Four parallel receive data lines. This data is driven by an external PHY that attached the media and should be synchronized with the **mii_rclk** signal.
mii_tclk	I	124	Supports the 25-MHz or 2.5-MHz transmit clock supplied by the external physical layer medium dependent (PMD) device. This clock should always be active.
mii_txd<3:0>	O	See Table 2.	Four parallel transmit data lines. This data is synchronized to the assertion of the **mii_tclk** signal and is latched by the external PHY on the rising edge of the **mii_tclk** signal.

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Table 4 (Cont.) Functional Description of DECchip 21142 Signals

Signal	Type	Pin Number	Description
mii_txen	O	123	Transmit enable signals that the transmit is active in the MII port to an external PHY device.
nc	O	86	No connection.
par	I/O	59	Parity is calculated by the 21142 as an even parity bit for the 32-bit **ad** and 4-bit **c_be_l** lines.
			During address and data phases, parity is calculated on all the **ad** and **c_be_l** lines whether or not any of these lines carry meaningful information.
pci_clk	I	19	The clock provides the timing for the 21142 related PCI bus transactions. All the bus signals are sampled on the rising edge of **pci_clk**. The clock frequency range is between 25 MHz and 33 MHz.
perr_l	I/O	57	Parity error asserts when a data parity error is detected.
			When the 21142 is the bus master and a parity error is detected, the 21142 asserts both CSR5 bit 13 (system error) and CFCS bit 8 (**serr_l** enable). Next, it completes the current data burst transaction, then stops operation. After the host clears the system error, the 21142 continues its operation.
			When the 21142 is the bus target and a parity error is detected, the 21142 asserts **perr_l**.
			This pin must be pulled up by an external resistor.
req_l	O	22	Bus request is asserted by the 21142 to indicate to the bus arbiter that it wants to use the bus.

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Table 4 (Cont.) Functional Description of DECchip 21142 Signals

Signal	Type	Pin Number	Description
rst_l	I	16	Resets the 21142 to its initial state. This signal must be asserted for at least 10 active PCI clock cycles. When in the reset state, all PCI output pins are put into tristate and all PCI O/D signals are floated.
serr_l	I/O	58	If an address parity error is detected and CFCS bit 31 (detected parity error) is enabled, 21142 asserts both **serr_l** (system error) and CFCS bit 30 (signal system error). When an address parity error is detected, system error asserts two clocks after the failing address. This pin must be pulled up by an external resistor.
sr_ck	O	114	Serial ROM clock signal.
sr_cs	O	115	Serial ROM chip-select signal.
sr_di	O	113	Serial ROM data-in signal.
sr_do	I	112	Serial ROM data-out signal.
stop_l	I/O	56	Stop indicator indicates that the current target is requesting the bus master to stop the current transaction. The 21142 responds to the assertion of **stop_l** when it is the bus master, either to disconnect, retry, or abort.
tck	I	11	JTAG clock shifts state information and test data into and out of the 21142 during JTAG test operations. This pin should not be left unconnected.
tdi	I	13	JTAG data in is used to serially shift test data and instructions into the 21142 during JTAG test operations. This pin should not be left unconnected.
tdo	O	14	JTAG data out is used to serially shift test data and instructions out of the 21142 during JTAG test operations.

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Table 4 (Cont.) Functional Description of DECchip 21142 Signals

Signal	Type	Pin Number	Description
tms	I	12	JTAG test mode select controls the state operation of JTAG testing in the 21142. This pin should not be left unconnected.
tp_rd–	I	10	Twisted-pair negative differential receive data from the twisted-pair lines.
tp_rd+	I	9	Twisted-pair positive differential receive data from the twisted-pair lines.
tp_td– **tp_td– –**	O O	5 4	Twisted-pair negative differential transmit data. The positive and negative differential transmit data outputs are resistively combined outside the 21142 with equalization to compensate for intersymbol interference on the twisted-pair medium.
tp_td+ **tp_td+ +**	O O	6 7	Twisted-pair positive differential transmit data. The positive and negative differential transmit data outputs are resistively combined outside the 21142 with equalization to compensate for intersymbol interference on the twisted-pair medium.
trdy_l	I/O	52	Target ready indicates the target agent's ability to complete the current data phase of the transaction. A data phase is completed on any clock when both **trdy_l** and **irdy_l** are asserted. Wait cycles are inserted until both **irdy_l** and **trdy_l** are asserted together. When the 21142 is the bus master, target ready is asserted by the bus slave on the read operation indicating that valid data is present on the **ad** lines. During a write cycle, it indicates that the target is prepared to accept data.
vcap_h	I	110	Capacitor input for analog phase-locked loop logic.
vdd	P	See Table 3.	3.3-V supply input voltage.

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Table 4 (Cont.) Functional Description of DECchip 21142 Signals

Signal	Type	Pin Number	Description
vddac	P	109, 111	Supplies +3.3-volt input for analog phase-locked loop logic.
vdd_clamp	P	20	Supplies +5 volts or +3.3 volts reference for clamp logic.
vss	P	See Table 3.	Ground pins.
xtal1	I	106	Crystal oscillator input.
xtal2	O	105	Crystal feedback output pin used for crystal connections only. If this pin is unused, then do not connect it.

2.2 Pin Tables

This section contains four types of pin tables:

- Table 5 lists the input pins.
- Table 6 lists the output pins.
- Table 7 lists the input/output pins.
- Table 8 lists the open drain pins.

Table 5 Input Pins

Signal	Active Level	Signal	Active Level
aui_cd–	Low	**mii_rxd<3:0>**	—
aui_cd+	High	**mii_tclk**	—
aui_rd–	Low	**pci_clk**	—
aui_rd+	High	**rst_l**	Low
gnt_l	Low	**sr_do**	High
idsel	High	**tck**	—
iref	High	**tdi**	—
mii_clsn	High	**tms**	High
mii_crs	High	**tp_rd–**	Low
mii_dv	High	**tp_rd+**	High
mii_rclk	—	**vcap_h**	High
mii_rx_err	High	**xtal1**	—

Table 6 Output Pins

Signal	Active Level	Signal	Active Level
aui_td–	Low	**req_l**	Low
aui_td+	High	**sr_ck**	—
br_a<0>	High	**sr_cs**	High
br_a<1>	High	**sr_di**	High
br_ce_l	Low	**tdo**	High
mii_mdc	—	**tp_td–**	Low
mii_txd<3:0>	—	**tp_td– –**	Low
mii_txen	High	**tp_td+**	High
nc	—	**tp_td+ +**	High
		xtal2	High

Table 7 Input/Output Pins

Signal	Active Level	Signal	Active Level
ad<31:0>	—	**gep<3>/10bt_link**	—
br_ad<7:0>	—	**irdy_l**	Low
c_be_l<3:0>	Low	**mii_mdio**	—
devsel_l	Low	**par**	—
frame_l	Low	**perr_l**	Low
gep<0>/aui_bnc	—	**serr_l**	Low
gep<1>/activ	—	**stop_l**	Low
gep<2>/rcv_match	—	**trdy_l**	Low

Table 8 Open Drain Pins

Signal	Active Level
int_l	Low

2.3 Signal Grouping by Function

Table 9 lists the signals according to their interface function.

Table 9 Signal Functions

Interface	Function	Signal
PCI	Address and data	**ad<31:0>**, **par**
	Arbitration	**gnt_l**, **req_l**
	Bus command and byte enable	**c_be_l<3:0>**
	Device select	**devsel_l**, **idsel**
	Error reporting	**perr_l**, **serr_l**
	Interrupt	**int_l**
	System	**pci_clk**, **rst_l**
	Control signals	**frame_l**, **stop_l**, **irdy_l**, **trdy_l**
MII network port	Transmit data lines	**mii_txd<3:0>**
	Receive data lines	**mii_rxd<3:0>**
	Transmit, receive clocks	**mii_tclk**, **mii_rclk**
	Transmit enable	**mii_txen**
	Collision detect	**mii_clsn**
	Error reporting	**mii_rx_err**
	Data control	**mii_dv**, **mii_crs**
	MII management data clock	**mii_mdc**
	MII management data input/output	**mii_mdio**
Test access port	JTAG test operations	**tck**, **tdi**, **tdo**, **tms**
Serial ROM port	Serial ROM	**sr_ck**, **sr_cs**, **sr_di**, **sr_do**
Boot ROM port	ROM interface	**br_a<1:0>**, **br_ad<7:0>**, **br_ce_l**

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Table 9 (Cont.) Signal Functions

Interface	Function	Signal
Power	3.3-V and 5.0-V supply input	**vdd**, **vddac**, **vdd_clamp**
	Ground	**vss**
General-purpose port and LEDs	General-purpose pins	**gep<3:0>**
	LED indicators	**activ**, **rcv_match**, **10bt_link**
	10BASE5/10BASE2 select	**aui_bnc**
Network connection	Analog phase-locked loop logic	**iref**, **vcap_h**
	AUI collision data	**aui_cd–**, **aui_cd+**
	AUI transmit and receive data	**aui_rd–**, **aui_rd+**, **aui_td–**, **aui_td+**
	Crystal oscillator	**xtal1**, **xtal2**
	Twisted-pair transmit and receive data	**tp_rd–**, **tp_rd+**, **tp_td–**, **tp_td– –**, **tp_td+**, **tp_td+ +**

3 Electrical and Environmental Specifications

This section contains the electrical and environmental specifications for the 21142.

Caution

Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21142. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21142.

3.1 Voltage Limit Ratings

Table 10 lists the voltage limit ratings.

Table 10 Voltage Limit Ratings

Parameter	Minimum	Maximum
Power supply voltage	+3.0 V	+3.6 V
vdd_clamp (5.0 V)	+4.75 V	+5.25 V
vdd_clamp (3.3 V)[1]	+3.0 V	+3.6 V
ESD protection voltage	—	2000 V

[1]In the 3.3 V signaling environment, **vdd_clamp** must not be greater than **vdd** + 0.3 V.

3.2 Temperature Limit Ratings

Table 11 lists the temperature limit ratings.

Table 11 Temperature Limit Ratings

Parameter	Minimum	Maximum
Storage temperature	–55°C	+125°C
Operating temperature	0°C	70°C

3.3 Supply Current and Power Dissipation

The values in Table 12 are estimates based on a PCI clock frequency of 33 MHz and a network data rate of 10Mb/s for SRL and 10/100Mb/s for MII.

Table 12 Supply Current and Power Dissipation

Symbol	Conditions	Typical	Maximum	Units
IDD	**vdd** =3.6 V, Ta=70°C	130	150	mA
Power	**vdd**=3.6 V, Ta=70°C	430	540	mW
Snooze mode power	VDD=3.6 V, Ta=70°C	180	225	mW
Sleep mode power	VDD=3.6 V, Ta=70°C	85	110	mW

3.3.1 PCI I/O Voltage Specifications

The 21142 meets the I/O voltage specifications listed in Table 13 and Table 14.

Table 13 I/O Voltage Specifications for 5.0-Volt Levels

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input high voltage	—	2.0 V	**vdd_clamp** + 0.5 V
Vil	Input low voltage	—	–0.5 V	0.8 V
Ii[1]	Input leakage current	0.5 V <Vin<2.7 V	—	±70 μA
Voh	Output high voltage	Iout=–2 mA	2.4 V	—
Vol[2]	Output low voltage	Iout=3 mA, 6 mA	—	0.55 V
Cap[3]	Pin capacitance	—	5 pF	8 pF

[1]Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

[2]Signals without pull-up resistors must have 3 milliamps low output current. Signals requiring pullup resistors (including **frame_l, trdy_l, irdy_l, devsel_l, stop_l, serr_l, and perr_l**) must have 6 milliamps.

[3]Parameter design guarantee.

Table 14 I/O Voltage Specifications for 3.3-Volt Levels

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input high voltage	—	0.475***vdd_clamp**	**vdd_clamp** + 0.5 V
Vil	Input low voltage	—	–0.5 V	0.325***vdd_clamp**
Ii[1]	Input leakage current	0.0 V <Vin<**vdd_clamp**	—	±70 µA
Voh	Output high voltage	Iout=–500 µA	0.9***vdd_clamp**	—
Vol	Output low voltage	Iout=1500 µA	—	0.1***vdd_clamp**
Cap[2]	Pin capacitance	—	5 pF	8 pF

[1]Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

[2]Parameter design guarantee.

3.3.2 PCI Reset

PCI reset (**pci_rst**) is an asynchronous signal that must be active for at least 10 active PCI clock (**pci_clk**) cycles. Figure 3 shows the PCI reset timing characteristics, and Table 15 lists the PCI reset signal limits.

Figure 3 PCI Reset Timing Diagram

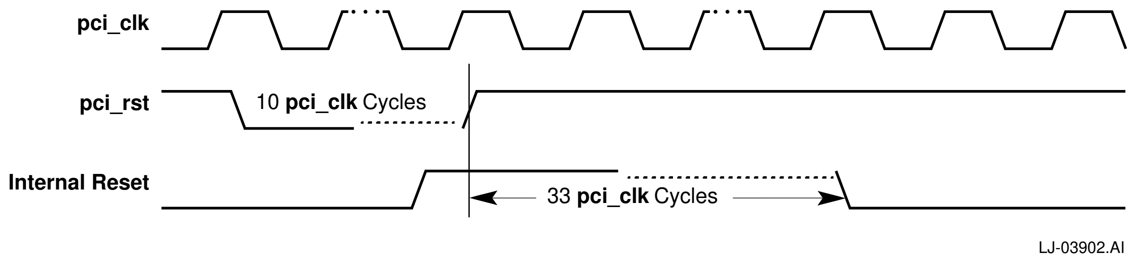


Table 15 PCI Reset Timing

Symbol	Parameter	Minimum	Maximum	Conditions
Trst	**pci_rst** pulse width	10*Tcycle	Not applicable	**pci_clk** active

3.3.3 PCI Clock Specifications

The clock frequency range[1] for the PCI is between 25 MHz and 33 MHz. Figure 4 shows the PCI clock specification timing characteristics and the required measurement points for both the 5.0-V and 3.3-V signaling environments. Table 16 lists the frequency-derived clock specifications.

Figure 4 PCI Clock Specifications Timing Diagram

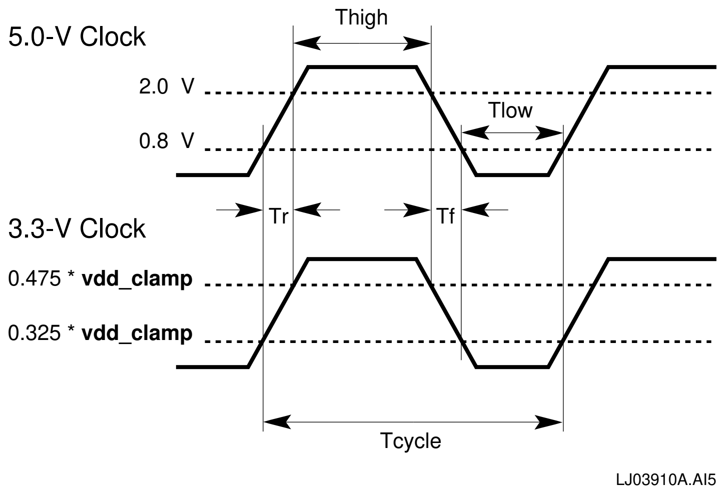


Table 16 PCI Clock Specifications

Symbol	Parameter	Minimum	Maximum
Tcycle	Cycle time	30 ns	50 ns
Thigh	**pci_clk** high time	11 ns	—
Tlow	**pci_clk** low time	11 ns	—
Tr/Tf[1]	**pci_clk** slew rate	1 V/ns	4 V/ns

[1]Rise and fall times are specified in terms of the edge rate measured in V/ns. Parameter design guarantee.

[1] The PCI clock frequency is from dc to 33 MHz; network operational with the PCI clock from 25 MHz to 33 MHz.

3.3.4 Other PCI Signals

Figure 5 shows the timing diagram characteristics, and Table 17 lists the other PCI signals. This timing is identical to the timing for the general-purpose register signals.

Figure 5 Timing Diagram for Other PCI Signals

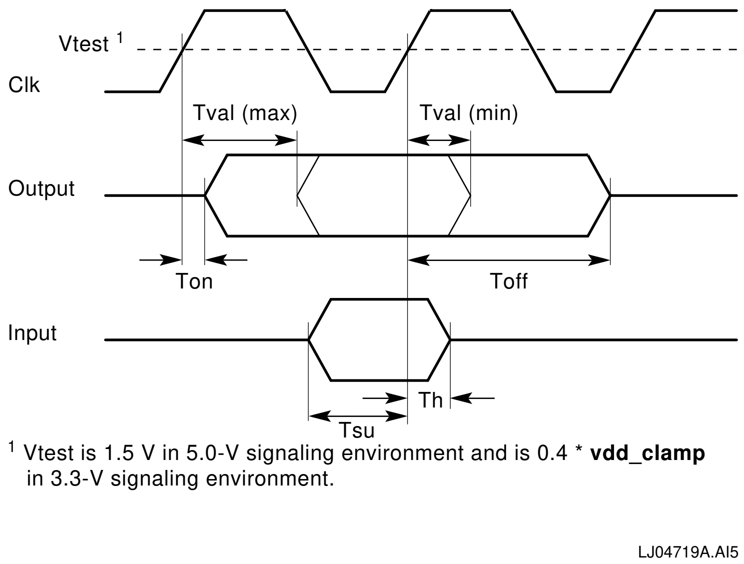


Table 17 Other PCI Signals

Symbol	Parameter	Minimum	Maximum
Tval[1]	clk-to-signal valid delay	2 ns	11 ns
Ton[2]	Float-to-active delay from clk	2 ns	—
Toff[2]	Active-to-float delay from clk	—	28 ns
Tsu	Input signal valid setup time before clk	7 ns	—
Th	Input signal hold time from clk	0 ns	—

[1]Load for this measurement is as specified in *PCI Local Bus Specification, Revision 2.0 and Revision 2.1*.

[2]Parameter design guarantee.

3.4 AUI and Twisted-Pair dc Specifications

Table 18 lists the dc specifications for the AUI and twisted-pair parts of the SIA.

Table 18 AUI and Twisted-Pair dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
AUI Pins					
V_{od}	Transmit differential output voltage (**aui_td±**)	78Ω termination	±550	±1200	mV
V_{odi}[1]	Transmit differential output idle voltage (**aui_td±**)	78Ω termination	–40	+40	mV
I_{odi}[1]	Transmit differential output idle current (**aui_td±**)	78Ω termination	–1	+1	mA
V_{asq+}[1]	Differential positive squelch threshold (**aui_rd±**)	—	175	275	mV
V_{asq-}[1]	Differential negative squelch threshold (**aui_rd±** and **aui_cd±**)	—	–275	–175	mV
V_{odu}[1]	Transmit differential output undershoot voltage on return to zero (**aui_td±**)	78Ω termination	—	–100	mV
Twisted-Pair Interface Pins					
V_{toh}	Output high voltage (**tp_td±** and **tp_td±±**)	I_{oh} = –25 mA	+ 2.5	V_{dd}	V
V_{tol}	Output low voltage (**tp_td±** and **tp_td±±**)	I_{ol} = 25 mA	V_{ss}	+ 0.5	V
V_{tsq+}[1]	Differential positive squelch threshold (**tp_rd±**)	—	300	520	mV
V_{tsq-}[1]	Differential negative squelch threshold (**tp_rd±**)	—	–520	–300	mV
V_{tdif}[1]	Differential input voltage range (**tp_rd±**)	—	–3.1	3.1	V

[1]Parameter design guarantee.

3.5 Serial Interface Attachment Specifications

This section describes the dc specifications and timing limits of the SIA unit.

3.5.1 Serial Clock Timing

Figure 6 shows the serial clock (TTL or CMOS) timing characteristics, and Table 19 lists the serial clock timing specifications.

Figure 6 Serial Clock (XTAL) Timing Diagram

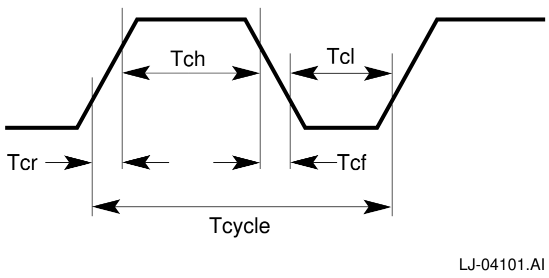


Table 19 Serial Clock (XTAL) Timing Specifications

Symbol	Parameter	Minimum	Maximum
Tcr[1]	Rise time	—	4 ns
Tcf[1]	Fall time	—	4 ns
Tcycle	Cycle time	49.995 ns	50.005 ns
Tch	Clock high time	0.4*Tcycle	0.6*Tcycle
Tcl	Clock low time	0.4*Tcycle	0.6*Tcycle

[1]Parameter design guarantee.

3.5.2 Internal SIA Mode AUI Timing—Transmit

Figure 7 shows the internal SIA transmit timing characteristics for the AUI, and Table 20 lists the internal SIA transmit timing limits for the AUI.

Figure 7 Internal SIA Mode AUI Timing Diagram—Transmit

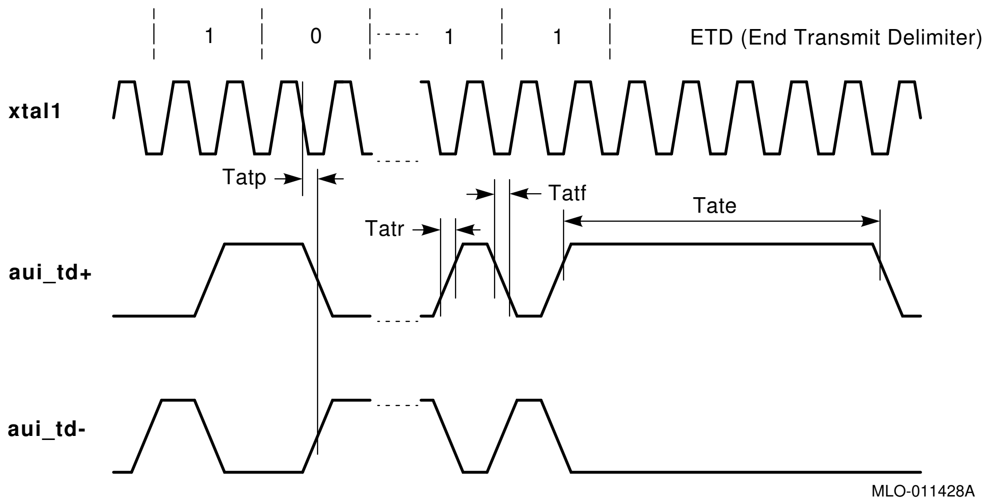


Table 20 Internal SIA Mode AUI Timing Specifications—Transmit

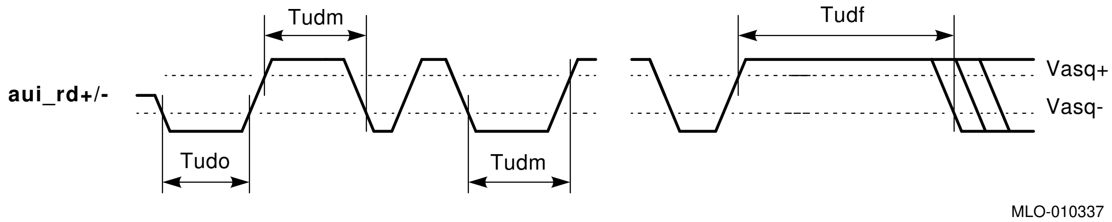
Symbol	Definition	Minimum	Maximum	Units
Tatp	**aui_td+, aui_td–** propagation delay from **xtal1** fall	—	30	ns
Tatr[1]	**aui_td+, aui_td–** rise time	2	8	ns
Tatf[1]	**aui_td+, aui_td–** fall time	2	8	ns
Tatm[1]	**aui_td+, aui_td–** rise and fall time mismatch (not shown)	—	1	ns
Tate	**aui_td±** end transmit delimiter length	345	405	ns

[1]Parameter design guarantee.

3.5.3 Internal SIA Mode AUI Timing—Receive

Figure 8 shows the internal SIA receive timing characteristics for the AUI, and Table 21 lists the internal SIA receive timing limits for the AUI.

Figure 8 Internal SIA Mode AUI Timing Diagram—Receive



3.5.4 Internal SIA Mode AUI Timing—Collision

Figure 9 shows the internal SIA collision timing characteristics for the AUI, and Table 21 lists the internal SIA collision timing limits for the AUI.

Figure 9 Internal SIA Mode AUI Timing Diagram—Collision

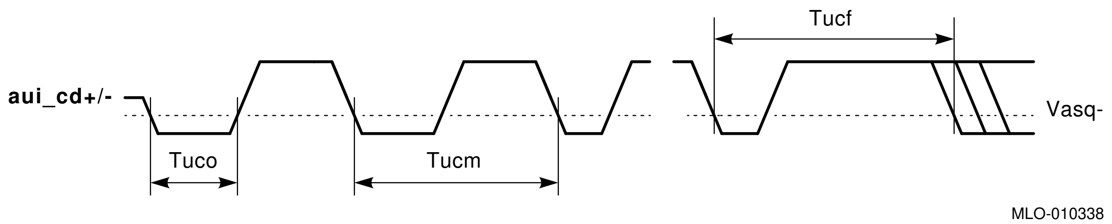


Table 21 Internal SIA Mode AUI Timing Specifications—Receive and Collision

Symbol	Definition	Minimum	Maximum	Units
Tudo	**aui_rd±** start of frame pulse width	15	20	ns
Tudm	**aui_rd±** delay between opposite squelch crossings not recognized as end of packet	—	140	ns
Tudf	**aui_rd±** delay from last squelch crossing recognized as end of packet	150	—	ns
Tuco	**aui_cd±** start of collision pulse width	20	25	ns
Tucm	**aui_cd±** delay between squelch crossings not recognized as end of collision	—	140	ns
Tucf	**aui_cd±** delay from last squelch crossing recognized as end of collision	150	—	ns

3.5.5 Internal SIA Mode 10BASE-T Interface Timing—Transmit

Figure 10 shows the internal SIA transmit timing characteristics for the 10BASE-T interface, and Table 22 lists the internal SIA transmit limits.

Figure 10 Internal SIA Mode 10BASE-T Interface Timing Diagram—Transmit

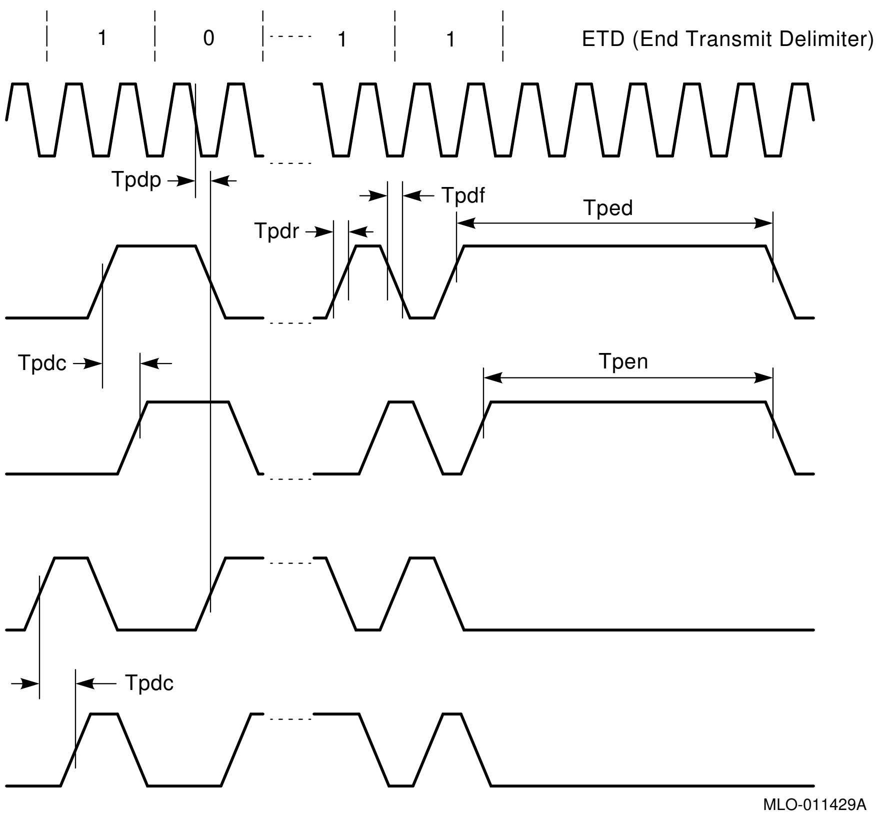


Table 22 Internal SIA Mode 10BASE-T Interface Timing Specifications—Transmit

Symbol	Definition	Minimum	Maximum	Units
Tpdp	**tp_td+, tp_td–** propagation delay from **xtal1** fall	—	30	ns
Tpdr[1]	**tp_td+, tp_td++, tp_td–, tp_td– –** rise time	2	8	ns
Tpdf[1]	**tp_td+, tp_td++, tp_td–, tp_td– –** fall time	2	8	ns
Tpdm[1]	**tp_td+, tp_td++, tp_td–, tp_td– –** rise and fall time mismatch (not shown)	—	1	ns
Tpdc	**tp_td+** to **tp_td– –** and **tp_td–** to **tp_td++** delay	46	54	ns
Tped	**tp_td±** end transmit delimiter length	295	355	ns
Tpen	**tp_td++/– –** end transmit delimiter length	245	305	ns

[1]Parameter design guarantee.

3.5.6 Internal SIA Mode 10BASE-T Interface Timing—Receive

Figure 11 shows the internal SIA receive timing characteristics for the 10BASE-T interface, and Table 23 lists the internal SIA receive limits for the 10BASE-T interface.

Figure 11 Internal SIA Mode 10BASE-T Interface Timing Diagram—Receive

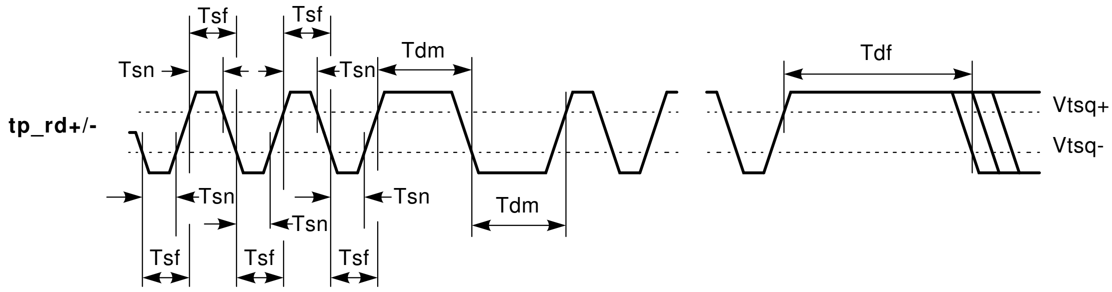


Table 23 Internal SIA Mode 10BASE-T Interface Timing Specifications—Receive

Symbol	Definition	Minimum	Maximum	Units
Tsn	**tp_rd±** start of frame pulse width during smart squelch operation	15	20	ns
Tsf	**tp_rd±** maximum delay between opposite squelch crossings not to turn smart squelch off	140	150	ns
Tdm	**tp_rd±** delay between opposite squelch crossings not recognized as end of packet	—	140	ns
Tdf	**tp_rd±** delay from last squelch crossing recognized as end of packet	150	—	ns

3.5.7 Internal SIA Mode 10BASE-T Interface Timing—Idle Link Pulse

Figure 12 shows the internal SIA idle link pulse timing characteristics for the 10BASE-T interface, and Table 24 lists the internal SIA idle link pulse limits for the 10BASE-T interface.

Figure 12 Internal SIA Mode 10BASE-T Interface Timing Diagram—Idle Link Pulse

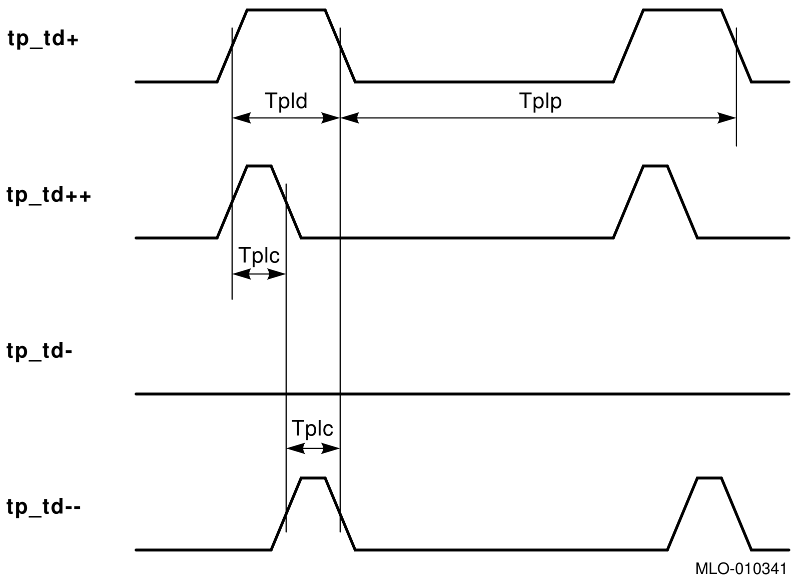


Table 24 Internal SIA Mode 10BASE-T Interface Timing Specifications—Idle Link Pulse

Symbol	Definition	Minimum	Maximum	Units
Tpld	**tp_td+** idle link pulse width	80	120	ns
Tplc	**tp_td++** and **tp_td– –** idle link pulse width	40	60	ns
Tplp	Idle link pulse period	8	24	ms

3.6 MII Interface Specifications

Table 25 lists the specifications for the MII interface.

Table 25 MII Interface

Symbol	Definition	Conditions	Minimum	Maximum	Units
V_{oh}	Output high voltage	I_{oh} = –4mA	2.4	—	V
V_{ol}	Output low voltage	I_{ol} = 4mA	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_{in}	Input current	V_{in} = V_{cc} or **vss**	–10.0	10.0	µA
I_{oz}	Maximum tristate output leakage current	V_{in} = **vdd** or **vss**	–10.0	10.0	µA

3.7 MII Port Timing

This section describes the MII port timing limits.

3.7.1 MII 10/100Mb/s and 10Mb/s Timing—Transmit

Figure 13 shows the MII port transmit timing characteristics, and Table 26 lists the MII port transmit timing limits.

Figure 13 MII Port Timing Diagram—Transmit

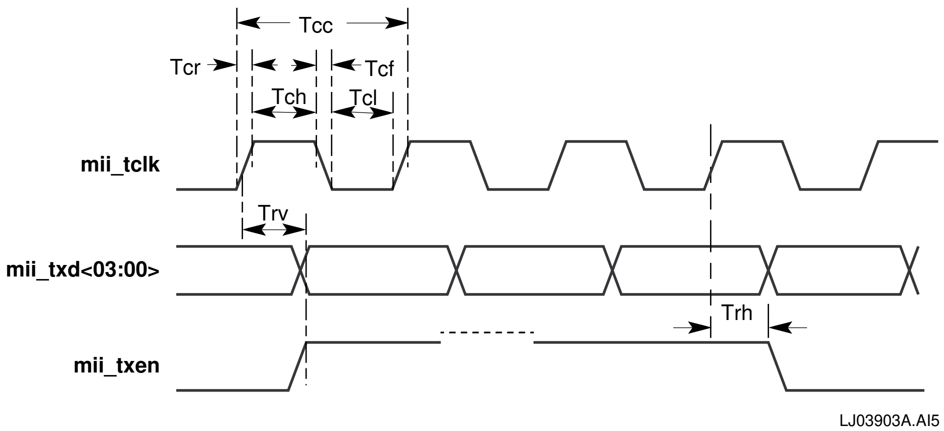


Table 26 MII Port Timing—Transmit

Symbol	Definition	Minimum	Typical	Maximum	Units
Tcc[1]	**mii_tclk** cycle time	—	40t[2]	—	ns
Tch	**mii_tclk** high time	10t[2]	—	26t[2]	ns
Tcl	**mii_tclk** low time	10t[2]	—	26t[2]	ns
Tcr	**mii_tclk** rise time	—	8	—	ns
Tcf	**mii_tclk** fall time	—	8	—	ns
Trv[3]	**mii_tclk** rise to **mii_txen** valid time or **mii_tclk** rise to **mii_txd** valid time	—	—	20	ns
Trh	**mii_txen** hold after **mii_tclk** rise time	5	—	—	ns

[1] ±50 parts per million.

[2] t=1 for 100Mb/s operation. t=10 for 10Mb/s operation.

[3] Outputs transmit data (**mii_txd**) and transmit enable (**mii_txen**) are driven internally from the rising edge of **mii_tclk**.

3.7.2 MII 10/100Mb/s Timing—Receive

Figure 14 shows the MII port receive timing characteristics, and Table 27 lists the MII port receive timing limits.

Figure 14 MII Port Timing Diagram—Receive

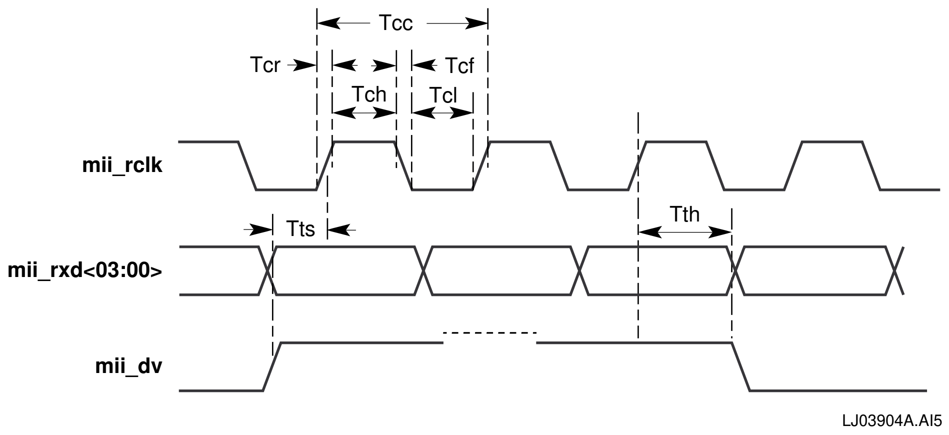


Table 27 MII Port Timing—Receive

Symbol	Definition	Minimum	Typical	Maximum	Units
Tcc[1]	**mii_rclk** cycle time	—	40t[2]	—	ns
Tch	**mii_rclk** high time	10t[2]	—	26t[2]	ns
Tcl	**mii_rclk** low time	10[2]	—	26t[2]	ns
Tcr	**mii_rclk** rise time	—	8	—	ns
Tcf	**mii_rclk** fall time	—	8	—	ns
Tts[3]	**mii_rxd** setup (both rise and fall transactions) to **mii_rclk** rise time or **mii_dv** setup (both rise and fall transactions) to **mii_rclk** rise time	10	—	—	ns
Tth	**mii_rxd** hold (both rise and fall transactions) after **mii_rclk** rise time or **mii_dv** hold (both rise and fall transactions) after **mii_rclk** rise time	10	—	—	ns

[1] ±50 parts per million.

[2] t=1 for 100Mb/s operation. t=10 for 10Mb/s operation.

[3] Inputs receive data (**mii_rxd**) and data valid (**mii_dv**) are latched internally on the rising edge of **mii_rclk**.

3.7.3 MII 10/100Mb/s Timing—Receive Error

Figure 15 shows the MII port receive error timing characteristics, and Table 28 lists the MII port receive error timing limits.

Figure 15 MII Port Timing Diagram—Receive Error

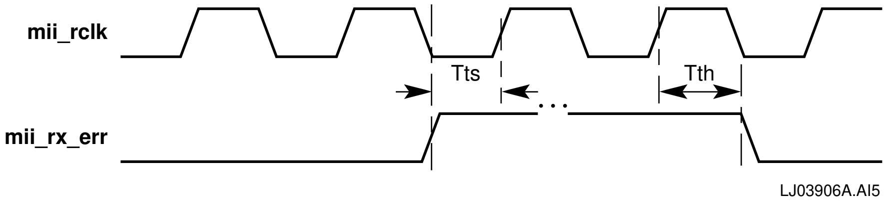


Table 28 MII Port Timing—Receive Error

Symbol	Definition	Minimum	Maximum	Units
Tts[1]	**mii_rx_err** setup (both rise and fall transactions) to **mii_rclk** rise time	10	—	ns
Tth[1]	**mii_rx_err** hold (both rise and fall transactions) after **mii_rclk** rise time	10	—	ns

[1]Input receive error (**mii_rx_err**) is latched internally on the rising edge of **mii_rclk**.

3.7.4 MII 10/100Mb/s Timing—Carrier Sense and Collision

Figure 16 shows the MII port carrier sense and collision timing characteristics, and Table 29 lists the MII port carrier sense and collision timing limits.

Figure 16 MII Port Timing Diagram—Carrier Sense and Collision

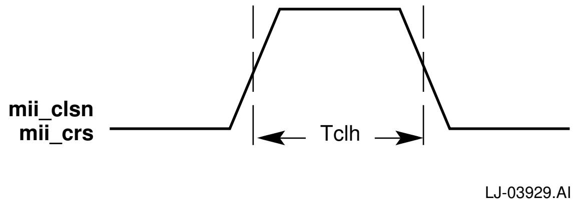


Table 29 MII Port Timing—Carrier Sense and Collision

Symbol	Definition	Minimum	Maximum	Units
Tclh	**mii_crs**, **mii_clsn** high time	20	—	ns

3.8 Boot ROM and Serial ROM Port Specification

Table 30 lists the dc specifications for the boot ROM and serial ROM ports. These specifications apply in any mode in which the ports are used.

Table 30 Boot ROM and Serial ROM Port dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
V_{oh}	Output high voltage	I_{oh} = –4 mA	2.4	—	V
V_{ol}	Output low voltage	I_{ol} = 4 mA	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_{oz}[1]	Maximum tristate output leakage current	V_{out} = **vdd** or **vss**	–10	10	μA

[1]For **sr_do** and **br_ce_l** the maximum value is 1000.0 μA.

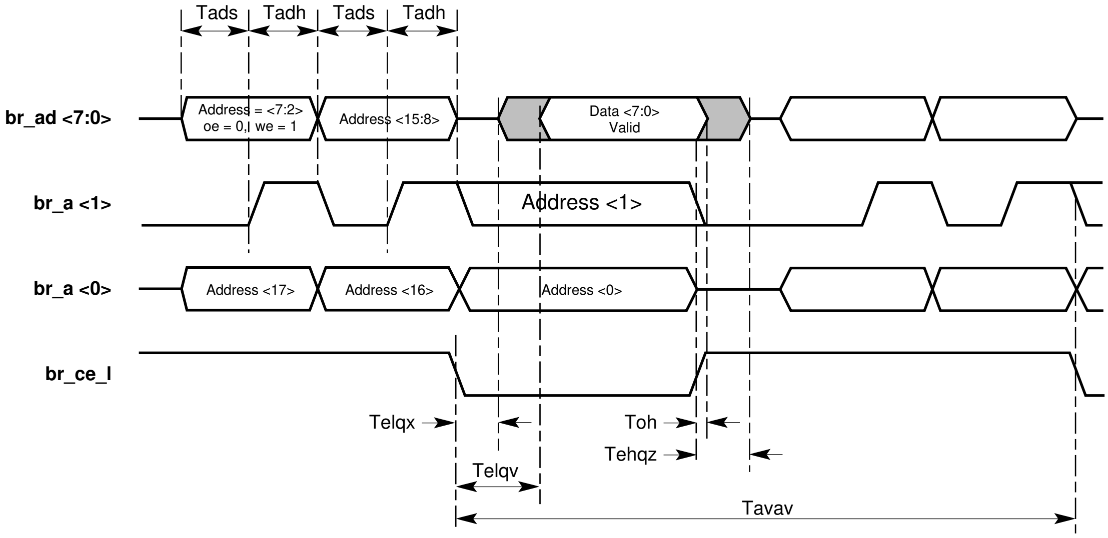
3.9 Boot ROM Port Timing

This section describes the boot ROM port timing.

3.9.1 Boot ROM Read Timing

Figure 17 shows the boot ROM read timing characteristics, and Table 31 lists the boot ROM read timing limits.

Figure 17 Boot ROM Read Timing Diagram



LJ-04104.AI

Table 31 Boot ROM Read Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Tavav	Read cycle time	120	—	ns
Tavqv	Address to output delay	—	120	ns
Telqv	**br_ce_l** to output delay	—	120	ns
Telqx[1]	**br_ce_l** to output low impedance	0	—	ns
Tehqz[1]	**br_ce_l** going high to output high impedance	—	55	ns
Toh	Output hold from **br_ce_l** change	0	—	ns
Tads	Address setup to latch enable high	30	—	ns
Tadh	Address hold from latch enable high	30	—	ns

[1]Parameter design guarantee.

3.9.2 Boot ROM Write Timing

Figure 18 shows the boot ROM write timing characteristics, and Table 32 lists the boot ROM write timing limits.

Figure 18 Boot ROM Write Timing Diagram

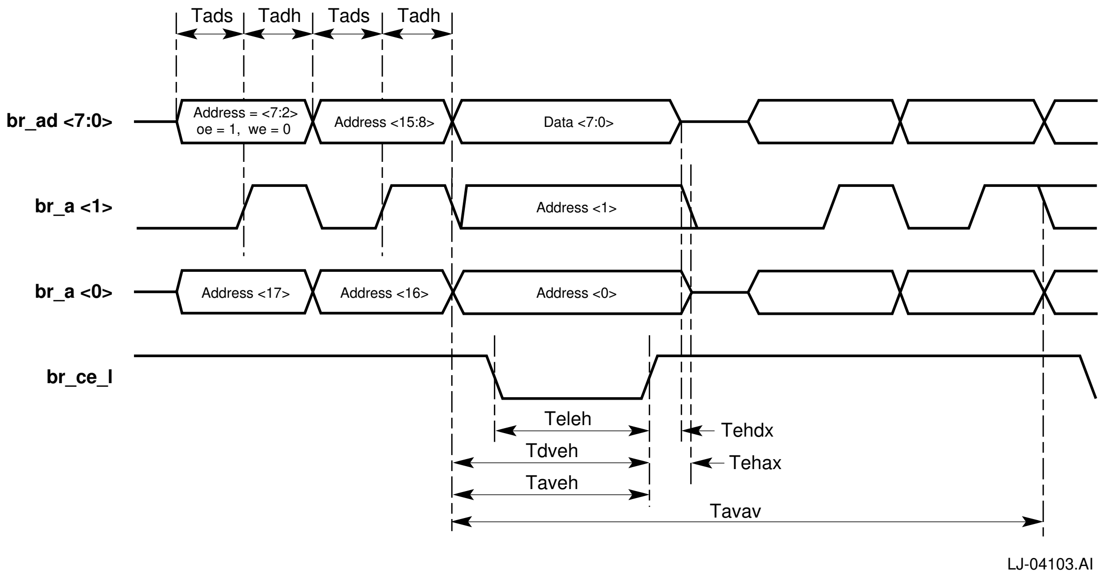


Table 32 Boot ROM Write Timing Specifications

Symbol[1]	Parameter	Minimum	Units
Tavav	Write cycle time	120	ns
Teleh	**br_ce_l** pulse width	70	ns
Taveh	Address setup to **br_ce_l** going high	50	ns
Tdveh	Data setup to **br_ce_l** going high	50	ns
Tehdx	Data hold from **br_ce_l** going high	10	ns
Tehax	Address hold from **br_ce_l** high	15	ns
Tads	Address setup to latch enable high	30	ns
Tadh	Address hold from latch enable high	30	ns

[1]There are no maximum specifications.

3.10 Serial ROM Port Timing

Figure 19 shows the serial ROM port timing, and Table 33 lists the characteristics. This timing is identical to the timing for the MII management signals (**mii_mdio** and **mii_mdc**).

Figure 19 Serial ROM Port Timing Diagram

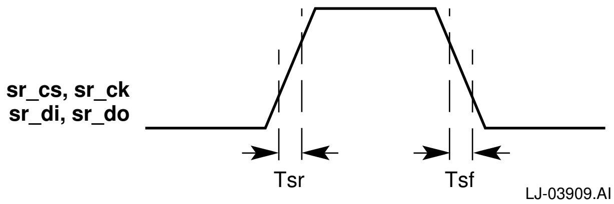


Table 33 Serial ROM Port Timing Characteristics

Symbol[1]	Definition	Maximum	Units
Tsr	Rise time	10	ns
Tsf	Fall time	10	ns

[1]There are no minimum specifications.

3.11 External Register Timing

Figure 20 shows the external register read timing characteristics, and Figure 21 shows its write timing characteristics. Table 34 lists the external register timing specifications for both read and write operations.

Figure 20 External Register Read Timing Diagram

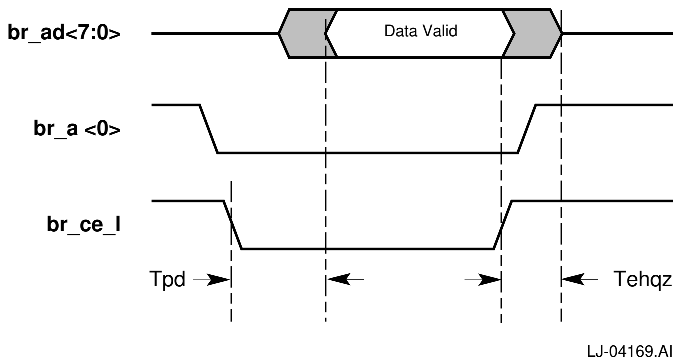


Figure 21 External Register Write Timing Diagram

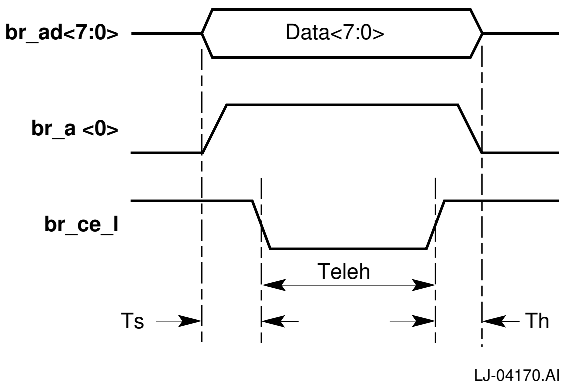


Table 34 External Register Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Teleh	**br_ce_l** pulse width	120	—	ns
Read Timing				
Tpd	**br_ce_l** low to **br_ad<7:0>** valid high	—	20	ns
Tehqz[1]	**br_ce_l** high to **br_ad<7:0>** high impedance	—	20	ns
Write Timing				
Ts	Data setup time prior to **br_ce_l**	30	—	ns
Th	Data hold after **br_ce_l** high	30	—	ns

[1]Parameter design guarantee.

3.12 Joint Test Action Group — Test Access Port

This section provides the joint test action group (JTAG) test access port specifications.

3.12.1 JTAG dc Specifications

Table 35 lists the dc specifications for the JTAG pins.

Table 35 JTAG dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
V_{oh}	Output high voltage	I_{oh} = –4 mA	2.4	—	V
V_{ol}	Output low voltage	I_{ol} = 4 mA	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_{ip}	Input leakage current on pins with internal pullups (**tck**, **tdi**, and **tms**)	0.0 <Vin<**vdd**	—	+20/–1000[1]	μA
I_{oz}	Tristate output leakage current (**tdo**)	0.0 <Vout<**vdd**	—	±20	μA

[1]For **tck**, **tdi**, and **tms** pins that have internal pullups, the leakage current can get to 1.0 mA when Vin = 0 V.

3.12.2 JTAG Boundary Scan Timing

Figure 22 shows the JTAG boundary scan timing, and Table 36 lists the interface signal timing relationships.

Figure 22 JTAG Boundary Scan Timing Diagram

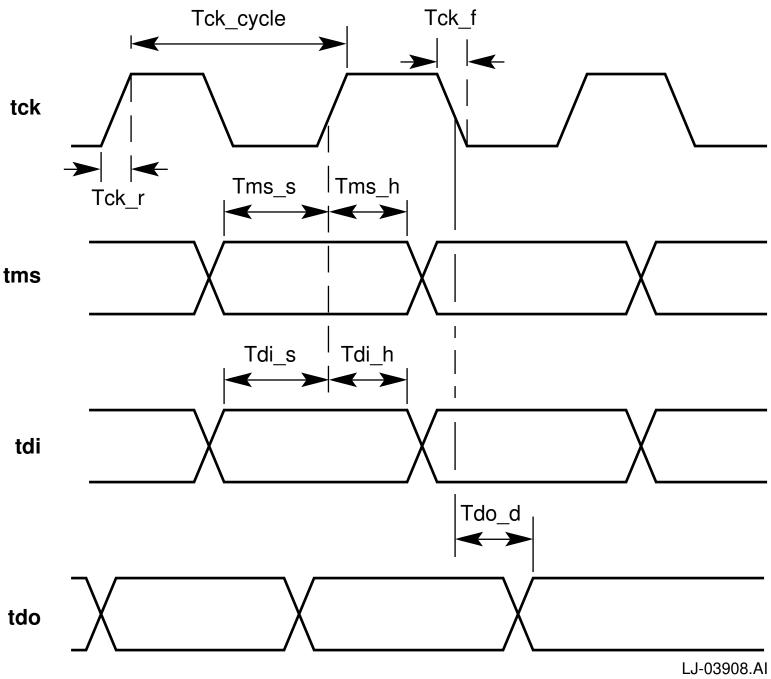


Table 36 JTAG Interface Signal Timing Relationships

Symbol	Parameter	Minimum	Maximum	Units
Tms_s	**tms** setup time	20	—	ns
Tms_h	**tms** hold time	5	—	ns
Tdi_s	**tdi** setup time	20	—	ns
Tdi_h	**tdi** hold time	5	—	ns
Tdo_d	**tdo** delay time	—	20	ns
Tck_r[1]	**tck** rise time	—	3	ns
Tck_f[1]	**tck** fall time	—	3	ns
Tck_cycle	**tck** cycle time	90	—	ns

[1]Parameter design guarantee.

4 Mechanical Specifications

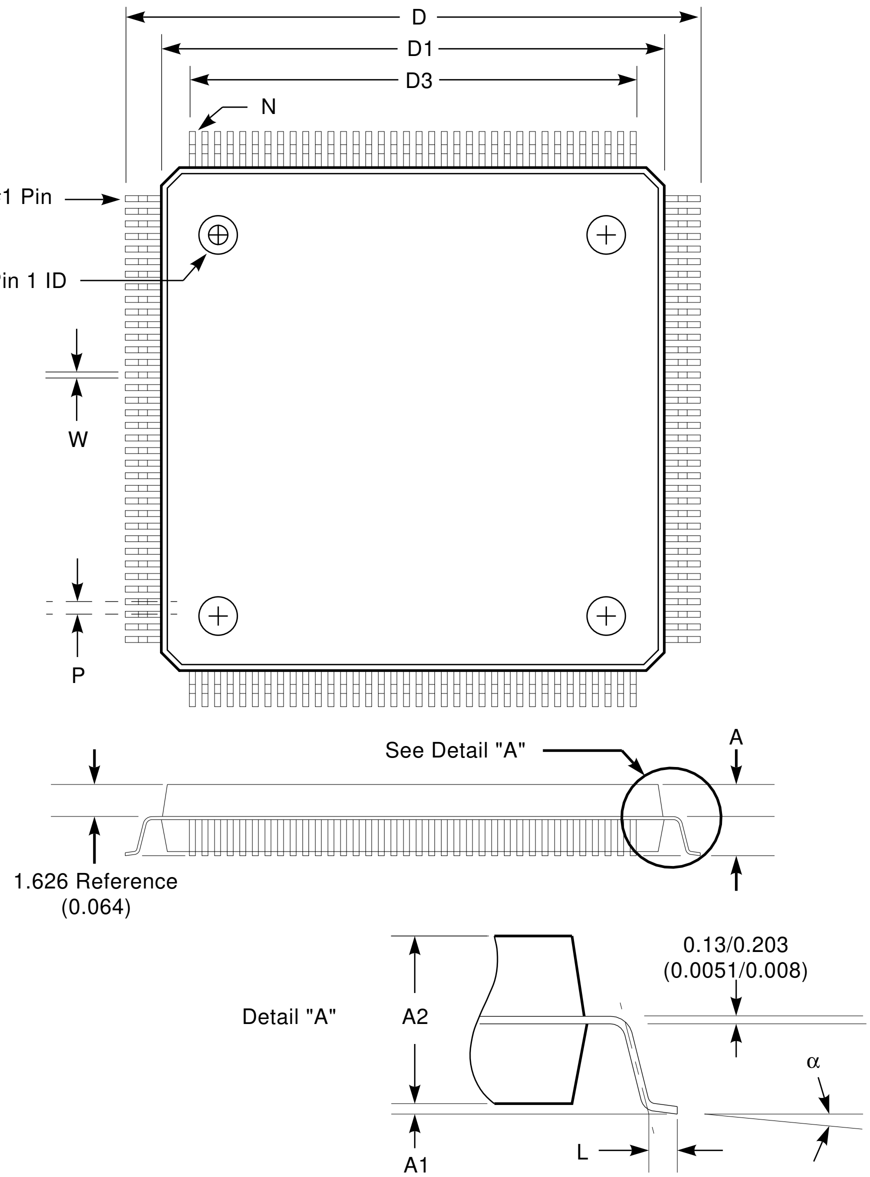
The 21142 is contained in a 144-pin PQFP. Table 37 lists the mechanical specifications, and Figure 23 shows the mechanical layout of the 21142.

Table 37 Mechanical Specifications

Item	Minimum[1]	Nominal[1]	Maximum[1]
A	—	—	4.07
A1	0.25	—	—
A2	3.17	3.37	3.67
D	—	31.20 BSC	—
D1	—	28.00 BSC	—
D3	22.75 Reference	22.75 Reference	22.75 Reference
L	0.65	0.80	1.00
N	—	144	—
P	0.59	0.65	0.71
W	0.22	0.30	0.38
α	0°	—	7°

[1]All dimensions (except α) are in millimeters.

Figure 23 Mechanical Layout of the DECchip 21142



Note: All dimensions (except α) are in millimeters.

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You can order the following semiconductor products from Digital:

Product	Order Number
DECchip PCI 21142 Fast Ethernet LAN Controller	21142–AA

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The following table lists some of the available Digital Semiconductor literature. For a complete list, contact the Digital Semiconductor Information Line.

Title	Order Number
DECchip 21142 PCI Fast Ethernet LAN Controller Product Brief	EC–QPNTA–TE

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