DECchip 21052 PCI-to-PCI Bridge Configuration:

An Application Note

Order Number: EC–QLZBA–TE

This application note presents guidelines for the configuration of the DECchip 21052 PCI-to-PCI Bridge in a system.

Revision/Update Information: This is a new application note.

Digital Equipment Corporation
Maynard, Massachusetts

July 1995

While Digital believes the information included in this publication is correct as of the date of publication, it is subject to change without notice.

Digital Equipment Corporation makes no representations that the use of its products in the manner described in this publication will not infringe on existing or future patent rights, nor do the descriptions contained in this publication imply the granting of licenses to make, use, or sell equipment or software in accordance with the description.

This document was prepared using VAX DOCUMENT Version 2.1.

Contents

Figures

Tables

1 Introduction

This document describes the configuration of the DECchip 21052 PCI-to-PCI Bridge (also referred to as the 21052) in a system. This application note is limited only to peripheral component interconnect (PCI) configuration of the 21052; it does not cover any hardware application topics. The following topics are included in this document:

- Summary of the 21052 configuration space
- Default state of the 21052 configuration space
- Initialization guidelines for the 21052
- Sample initializations

2 Functional Overview

The DECchip 21052 PCI-to-PCI Bridge connects two independent PCI buses. You can implement the 21052 either on a motherboard to provide capability for additional slots and devices, or on an add-in card to allow for multiple devices. You can also use the 21052 to isolate bus traffic.

The 21052 is a transparent device, that is, it requires no special driver software to run in a system. The 21052 does require initialization code to set up its configuration space, allocate memory and I/O space behind the bridge, identify VGA devices behind the 21052, and so on. This initialization code resides in the system BIOS or firmware.

Once configured, the 21052 operates without the need for any additional software control.

3 DECchip 21052 Configuration Space

The configuration registers of the 21052 comply with the registers of the Type 1 configuration header format for PCI-to-PCI bridges, as specified in the *PCI-to-PCI Bridge Architecture Specification*. The first 16 bytes of this header are identical to those of any other PCI device. The remaining 48 bytes of the predefined header are specific to the PCI-to-PCI bridge architectural standard.

The 21052 also implements 16 bytes of implementation-specific configuration space header. For a detailed description of each field, refer to the *DECchip 21052 PCI-to-PCI Bridge Data Sheet*.

Figure 1 shows a configuration space map for the 21052.

Figure 1 DECchip 21052 Configuration Space Map

31 24	23 16	15 08	07 00	Offset
Device ID		Vendor ID		00h
Primary Status		Primary Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Primary Latency Timer	Cache Line Size	0Ch
Reserved				10h
Reserved				14h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		I/O Limit	I/O Base	1Ch
Memory Limit		Memory Base		20h
Prefetchable Memory Limit		Prefetchable Memory Base		24h
Reserved				28h
Reserved				2Ch
Reserved				30h
Reserved				34h
Reserved				38h
Bridge Control		Interrupt Pin	Reserved	3Ch
p_serr_l Event Disable	Burst Limit Counter	Diagnostic Control	Chip Control	40h
Reserved		Secondary Target Wait Timer	Primary Target Wait Timer	44h
Secondary Write Attempt Counter				48h
Primary Write Attempt Counter				4Ch
Reserved				50h - FFh

LJ-04466.AI5

Table 1 provides the bit definitions of 21052 control registers. For a description of these bits, refer to the *DECchip 21052 PCI-to-PCI Bridge Data Sheet*.

Table 1 Bit Definitions

Field Bit	DWord Bit	Description
		Primary Command (Dword Offset 04h)
0	0	I/O enable
1	1	Memory enable
2	2	Master enable
3	3	Reserved
4	4	VGA snoop enable
5	5	Parity error response
6	6	Wait cycle control
7	7	**p_serr_l** driver enable
8	8	Fast back-to-back control
15:9	15:9	Reserved
		Secondary Status (Dword Offset 1Ch)
6:0	22:16	Reserved
7	23	Fast back-to-back capable
8	24	Data parity detected
10:9	26:25	**s_devsel_l** timing
11	27	Signaled target abort
12	28	Received target abort
13	29	Received master abort
14	30	Detected system error
		Chip Control (Dword Offset 40h)
0	0	Arbitration mode
1	1	Disable posting
3:2	3:2	Request mask timer
4	4	Secondary prefetch enable

(continued on next page)

Table 1 (Cont.) Bit Definitions

Field Bit	DWord Bit	Description
Primary Status (Dword Offset 06h)		
6:0	22:16	Reserved
7	23	Fast back-to-back capable
8	24	Data parity detected
10:9	26:25	**p_devsel_l** timing
11	27	Signaled target abort
12	28	Received target abort
13	29	Received master abort
14	30	Signaled system error
15	31	Detected parity error
Bridge Control (Dword Offset 3Ch)		
0	16	Parity error response
1	17	**s_serr_l** forward enable
2	18	ISA enable
3	19	VGA enable
4	20	Reserved
5	21	Master abort mode
6	22	Secondary bus reset
7	23	Fast back-to-back control
15:8	31:24	Reserved
Diagnostic Control (Dword Offset 41h)		
0	8	Chip reset
1	9	Test mode
2	10	**p_perr_l** diagnostic assertion
3	11	**s_perr_l** diagnostic assertion
4	12	**p_serr_l** diagnostic assertion
7:5	15:13	Reserved
p_serr_l Disable (Dword Offset 43h)		
0	24	Reserved
1	25	Bad data parity on target bus for posted write
2	26	Unable to deliver posted write data
3	27	Target abort on target bus during posted write
4	28	Master abort on target bus during posted write
7:5	31:29	Reserved

4 DECchip 21052 Initial Conditions

After system reset, the 21052 is initialized to the following state:

- Memory, I/O, and master enables all reset to zero. The 21052 does not respond to any memory or I/O transaction on either the primary or secondary bus.
- Primary, secondary, and subordinate bus numbers are all 0. You must initialize these bus numbers before you can configure any devices downstream of the 21052.
- Prefetchable memory, nonprefetchable memory, and I/O base and limit address registers are all 0. This does not mean that these address ranges are turned off. In fact, a memory range of addresses 000FFFFF (hex)–00000000 (hex) and an I/O range of addresses 0FFF (hex)–0000 (hex) are defined for downstream forwarding; however, because the enables are off, no memory or I/O transactions are forwarded. Before turning on those enables, it is very important that you initialize these address ranges. To turn off downstream forwarding, set the address base to a value greater than the address limit.
- All master latency and target wait timers are set to 0, which means that no limits are imposed. The implementation-specific burst count is set to 0, so no burst count limits are imposed.
- Cache line size is set to 0. No cache line boundaries are observed, and memory write and invalidate commands are forwarded as memory write commands.
- Parity checking, **p_serr_l** assertion, VGA modes, and ISA modes are all disabled.
- All device-specific features are disabled (reset to 0).

5 System Initialization

The *PCI-to-PCI Bridge Architecture Specification* provides guidelines for initialization. Some of this information is included here to aid initialization code development.

When the 21052 or any other PCI-to-PCI bridge is present in a system, either on the system board or on a PCI add-in card, system BIOS is required to provide the following functions during the initialization process:

- Assigning PCI bus numbers
- Allocating address ranges (prefetchable memory, nonprefetchable memory, and I/O)
- Writing the interrupt request (IRQ) number into each device
- Initializing the PCI display subsystem

6 Assigning PCI Bus Numbers

The system BIOS must assign PCI bus numbers to each PCI-to-PCI bridge in the system. The order and when the PCI bus numbers are assigned is not specified. The following requirements must be followed:

- All buses located downstream of a PCI-to-PCI bridge must reside between the secondary bus number and the subordinate bus number (inclusive).
- Bus number ranges in parallel branches of PCI bus hierarchy must be mutually exclusive.

7 Allocating Address Ranges

The system BIOS must map all devices residing behind the bridge into one of the 21052 address ranges. Address ranges supported by the 21052 are I/O space, prefetchable memory, and nonprefetchable memory (also called memory-mapped I/O). The address ranges have the following characteristics:

Address Range	Maximum Range	Minimum Granularity
I/O	64KB	4KB
Prefetchable memory	4GB	1MB
Nonprefetchable memory (memory-mapped I/O)	4GB	1MB

Because the 21052 has only one window for each address type, the system BIOS must group all devices that use a particular address space into a single window. The address range of a 21052 must include the same type of address range of all the PCI-to-PCI bridges and devices behind it.

To minimize wasted space, particularly in memory space, Digital recommends that you map larger memory requests before smaller memory requests. Devices must be mapped on a size-aligned boundary.

8 Mapping I/O Space Using ISA Mode

When an ISA or EISA bus is in the system, I/O space can become fragmented. An ISA address uses only 10 bits of addressing, giving a maximum 1KB of address space. Because ISA devices decode only the lowest 10 bits, these addresses are aliased throughout the entire I/O space. The bottom 256 bytes of a 1KB chunk point to system-specific addresses. The top 768 bytes are used for general I/O. EISA systems use the entire 64KB space by dividing the space into 16 4KB slots, and use a slot-specific control strobe to point to a particular slot. Slot 0 is generally allocated to the motherboard.

PCI-to-ISA and PCI-to-EISA bridges typically perform full 32-bit addressing, using positive decoding for the bottom 256 bytes of the first 1K chunk and subtractive decoding for the upper 768 bytes of each 1K chunk. Although the top 768 bytes of each chunk might be used for general ISA/EISA devices, the bottom 256 bytes in all slots but slot 0 (the bottom 4K slots) are available for use by PCI devices.

The 21052 provides a mode that allows mapping into the low 256 bytes of each 1K chunk. When ISA mode on the 21052 is set, it forwards only downstream transactions addressing the low 256 bytes of each 1K chunk inside the defined address range. This allows you to map PCI devices into I/O space when there is an ISA or EISA bus in the system. When mapping a device downstream of the 21052 with ISA mode set, bits <9:8> of the device's I/O base address should be 00.

9 Using the 21052 VGA Modes

You can configure the 21052 to support VGA-compatible devices.

When a VGA-compatible device is located downstream of a PCI-to-PCI bridge, set the VGA mode bit in 21052 configuration space in every PCI-to-PCI bridge between the device and the most primary PCI bus. Setting this bit configures the 21052 to pass all VGA frame buffer memory addresses and all VGA I/O addresses downstream.

When a graphics device that does not have VGA-compatibility is located downstream of the 21052, you must configure the bridge to forward only VGA palette writes by setting the VGA snoop bit in the 21052 configuration space. Again, you must set this bit in every PCI-to-PCI bridge between the most primary PCI bus and the graphics device.

If both types of devices are located downstream of the 21052, setting the VGA mode bit is sufficient for proper operation; however, setting both the VGA mode and the VGA snoop bits results in the same behavior as setting only the VGA mode bit.

For more information about VGA support in PCI systems, refer to the *PCI-to-PCI Bridge Architecture Specification*.

10 Sample 21052 Initializations

This section provides several sample initializations of the 21052.

10.1 Initializing the 21052 for Hierarchical Configuration Accesses

To initialize the 21052 so that configuration transactions can be forwarded, write the following bridge configuration registers (values in hex):

Dword Offset	Register	Value	Notes
04h	Primary status/ command	FFFF0000h	Clear all status bits. Make sure memory, I/O, and master enables are off.
18h	Subordinate/ secondary/primary bus numbers	00*xxyyzz*h	*xx* = Subordinate bus number *yy* = Secondary bus number *zz* = Primary bus number

The important points are:

- Turn off memory, I/O, and master enables to prevent memory and I/O transactions from crossing the bridge.
- Initialize PCI bus numbers for forwarding of configuration transactions across the bridge.

10.2 Initializing the 21052 for I/O and Configuration Forwarding

To initialize the 21052 so that I/O and configuration transactions can be forwarded, write the following bridge configuration registers (values in hex):

Dword Offset	Register	Value	Notes
18h	Subordinate/ secondary/primary bus numbers	00*xxyyzz*h	*xx* = Subordinate bus number *yy* = Secondary bus number *zz* = Primary bus number
1Ch	Secondary status/ I/O limit address/ I/O base address	FFFF*x*0*y*0h	Clear status bits. *x* = I/O limit address bits <15:12> *y* = I/O base address bits <15:12>
20h	Memory limit/ memory base	0000FFFFh	Turn off downstream memory address range.
24h	PF memory limit/ PF memory base	0000FFFFh	Turn off downstream PF memory address range.
3Ch	Bridge control	000*x*0000h	*x* = 0: no ISA bus in system *x* = 4: ISA bus in system
04h	Primary status/ command	FFFF0005h	Clear status bits. Turn on I/O enable for downstream I/O. Turn on master enable for upstream I/O. Write this register last.

The important points are:

- Initialize PCI bus numbers for forwarding of configuration transactions across the bridge.
- Initialize I/O base and limit registers to define a downstream window.
- Turn off both memory ranges.
- If an (E)ISA bus is in the system, turn on ISA mode.
- Turn on I/O and master enables (write this register last).

Note

Setting the master enable bit also enables forwarding of memory transactions upstream.

10.3 Initializing the 21052 for Memory and Configuration Forwarding

To initialize the 21052 so that memory and configuration transactions can be forwarded, write the following bridge configuration registers (values in hex):

Dword Offset	Register	Value	Notes
18h	Subordinate/ secondary/primary bus numbers	00*xxyyzz*h	*xx* = Subordinate bus number *yy* = Secondary bus number *zz* = Primary bus number
1Ch	Secondary status/ I/O limit address/ I/O base address	FFFF00FFh	Clear status bits. Turn off I/O address range.
20h	Memory limit/ memory base	*xxx* 0*yyy*0h	*xxx* = Nonprefetchable memory limit address <31:20> *yyy* = Nonprefetchable memory base address <31:20> To disable this range, write 0000FFFFh.
24h	PF memory limit/ PF memory base	*xxx*0*yyy*0h	*xxx* = Prefetchable memory limit address <31:20> *yyy* = Prefetchable memory base address <31:20> To disable this range, write 0000FFFFh.
04h	Primary status/ command	FFFF0006h	Clear status bits. Turn on memory enable for downstream memory. Turn on master enable for upstream memory. Write this register last.

The important points are:

- Initialize PCI bus numbers for forwarding of configuration transactions across the bridge.
- Turn off I/O range.
- Initialize either or both nonprefetchable and prefetchable memory ranges.
- Turn on memory and master enables (write this register last).

Note

Setting the master enable bit also enables forwarding of the I/O transactions upstream.

10.4 Initializing the 21052 for Memory, I/O, and Configuration Forwarding

To initialize the 21052 so that memory, I/O, and configuration transactions can be forwarded, write the following bridge configuration registers (values in hex):

Dword Offset	Register	Value	Notes
18h	Subordinate/ secondary/primary bus numbers	00*xxyyzz*h	*xx* = Subordinate bus number *yy* = Secondary bus number *zz* = Primary bus number
1Ch	Secondary status/ I/O limit address/ I/O base address	FFFF*x*0*y*0h	Clear status bits. *x* = I/O limit address bits <15:12> *y* = I/O base address bits <15:12>
20h	Memory limit/ memory base	*xxx*0*yyy*0h	*xxx* = Nonprefetchable memory limit address <31:20> *yyy* = Nonprefetchable memory base address <31:20> To disable this range, write 0000FFFFh.
24h	PF memory limit/ PF memory base	*xxx*0*yyy*0h	*xxx* = Prefetchable memory limit address <31:20> *yyy* = Prefetchable memory base address <31:20> To disable this range, write 0000FFFFh.
3Ch	Bridge control	000*x*0000h	*x* = 0: no ISA bus in system *x* = 4: ISA bus in system
04h	Primary status/ command	FFFF0007h	Clear status bits. Turn on I/O enable for downstream I/O. Turn on memory enable for downstream memory. Turn on master enable for upstream memory and I/O. Write this register last.

The important points are:

- Initialize PCI bus numbers for forwarding of configuration transactions across the bridge.
- Initialize the I/O range.
- Initialize either or both nonprefetchable and prefetchable memory ranges.
- Turn on memory and master enables (write this register last).

11 Initializing VGA Modes in the 21052

The following sections provide examples of initializing VGA mode and VGA snoop mode.

11.1 VGA Mode

If a VGA device resides behind the 21052, enable VGA mode. To enable VGA mode, write bit 18 of configuration address 3Ch. Simply modify the contents of the write to this register shown in previous sections. For example:

Dword Offset	Register	Value	Notes
3Ch	Bridge control	000*x*0000h	*x* = 8: VGA mode, no ISA bus in system *x* = C: VGA mode, ISA bus in system

You must write this register before memory, I/O, and master enables located at configuration address 04h are set.

11.2 VGA Snoop Mode

If a graphics device requiring VGA snoop mode resides behind the 21052, you must write bit 5 of configuration address 04h. Simply modify the contents of the write to this register shown in previous sections. For example:

Dword Offset	Register	Value	Notes
04h	Primary status/ command	FFFF002*x*h	*x* = 7: Set memory, I/O, and master enable (if all memory and I/O ranges are used) *x* = 5: Set I/O and master enable (if only the I/O range is used)

12 Initializing Optional Registers in the 21052

This section describes initialization of optional 21052 features. The features are not required for basic bridge operation. It is recommended that you write these registers before (or in the same access as) setting the memory, I/O, and master enables in configuration address 04h. Otherwise, order is not important.

12.1 Enabling Parity and Checking Errors

The following table lists the accesses to enable parity checking on both interfaces and to forward **serr#** from the secondary to the primary interface.

Dword Offset	Register	Value	Notes
3Ch	Bridge control	000*x*0000h	*x* = 3: No ISA bus in system, no VGA behind 21052 *x* = 7: ISA bus in system, no VGA behind 21052 *x* = B: No ISA bus in system, VGA behind 21052 *x* = F: ISA bus in system, VGA behind 21052
04h	Primary status/ command	FFFF01*xy*h	Clear status bits. *x* = 4: No VGA snoop mode *x* = 6: VGA snoop mode *y* = [0,5,6,7]: [configuration only, I/O only, memory only, all] enabled for downstream forwarding Write this register last.

12.2 Enabling Timers and Setting Cache Line Size

The following table lists the accesses to enable the master latency timers, the target wait timers, and the burst count to desired values. The setting of cache line size is also shown. Writing a value of 0 disables the timers and cache line size.

Dword Offset	Register	Value	Notes
0Ch	Primary MLT/cache line size	0000*xxyy*h	*xx* = Primary master latency timer value (low 3 bits = 0) *yy* = Cache line size
18h	Secondary MLT/ subordinate/ secondary/primary bus numbers	*wwxxyyzz*h	*ww* = Secondary master latency timer value (low 3 bits = 0) *xx* = Subordinate bus number *yy* = Secondary bus number *zz* = Primary bus number
40h	Burst control limit/ chip control	00*xx*0000h	*xx* = Burst count limit (top 2 bits = 0)
44h	Secondary wait timer/primary wait timer	0000*xxyy*h	*xx* = Secondary wait timer value *yy* = Primary wait timer value

12.3 Enabling Request Mask Timer and Posting Disable

The following table lists implementation-specific options you can select by writing bits in the chip control register (configuration address 40h).

Field	Feature	Value	Notes
<0>	Secondary arbitration mode	00000001h	Enable arbiter to perform in strict rotation mode. Disable posting.
<3:2>	Request mask timer	0000000*x*h	*x*<3:2>: Encoded timer value. *x* = 0h: Timer disabled *x* = 4h: 16 PCI clocks *x* = 8h: 32 PCI clocks *x* = Ch: 64 PCI clocks

13 Technical Support, Ordering, and Associated Literature

This section describes how to obtain information and technical support, as well as how to order Digital's products and associated literature.

13.1 Digital Semiconductor Information Line

If you need technical support or help deciding which literature best meets your needs, call the Digital Semiconductor Information Line:

United States and Canada	**1–800–332–2717**
TTY (United States only)	**1–800–332–2515**
Outside North America	**+1–508–568–6868**

13.2 Ordering Digital Semiconductor Products

To order the following Digital Semiconductor products, contact your local Digital sales office or local distributor.

Product	Order Number
DECchip 21052 PCI-to-PCI Bridge	21052–AA

13.3 Ordering Associated Literature

The following table lists the DECchip 21052 literature that is available. For ordering information, contact the Digital Semiconductor Information Line.

Title	Order Number
DECchip 21052 PCI-to-PCI Bridge Data Sheet	EC–QHURA–TE
DECchip 21052 PCI-to-PCI Bridge Product Brief	EC–QHUQA–TE
DECchip 21052 PCI-to-PCI Bridge Evaluation Board User's Guide	EC–QKHJA–TE
DECchip 21052 PCI-to-PCI Bridge Hardware Implementation: An Application Note	EC–QLZAA–TE

13.4 Ordering Third-Party Literature

You can order the following third-party literature directly from the vendor.

Title	Vendor
PCI Local Bus Specification, Revision 2.0 PCI-to-PCI Bridge Architecture Specification, Revision 1.0	PCI Special Interest Group M/S HF3–15A 5200 NE Elam Young Pkwy Hillsboro, OR 97124–6497 (503) 696–2000