Connecting the DECchip 21041 PCI Ethernet LAN Controller to the Network:

An Application Note

Order Number: EC–QJBWA–TE

This application note provides information necessary to implement network connections to the 21041 Ethernet LAN controller. Connections can be made to CPUs with a direct connection to an onboard peripheral component interconnect (PCI) bus, or to CPUs without a direct PCI connection by using a bus-to-bus interface.

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Implementing Network Connections

1 Overview

This application note describes how to implement network connections to the DECchip 21041 Ethernet LAN controller (21041). Its primary objective is to achieve an error-free implementation of the Ethernet network interface. This application note describes only hardware implementations, providing hardware designs and layout rules.

For detailed technical product requirements, the product developer should refer to the *DECchip 21041 PCI Ethernet LAN Controller Data Sheet* and the *DECchip 21041 PCI Ethernet LAN Controller Hardware Reference Manual*.

2 Functional Overview

This section provides an overview of the system and network interfaces.

2.1 System Interface

The 21041 has a single 50-pin connection, which consists of the control and address/data signals of a PCI bus.

The 21041 provides complete implementation of the IEEE 802.3 Ethernet specification from the attachment unit interface (AUI) and the twisted-pair (10BASE-T) interface through the media access control (MAC) layer, and creates a direct interface to the PCI bus. The PCI interface operates on the bus and uses approximately 1% of the bus bandwidth during an Ethernet reception or transmission. The bus master design provides for high throughput between the system and the network, yet it requires only a minimum of components for a complete implementation.

2.2 Network Interface

The 21041 physical layer design supports AUI drop cable Ethernet and 10BASE-T twisted-pair (TP) Ethernet connections. The 21041 **AUI_BNC** pin 92 provides for a connection of either the AUI (10BASE-5) or BNC (10BASE2) network connector. This pin is controlled by software and when programmed to a one, the AUI port is selected, disabling the BNC transceiver (or dc-to-dc converter). When this pin is programmed to zero, the BNC port is selected, enabling the BNC transceiver.

AUI signals interface with the Manchester encoder/decoder portion of the 21041. The 21041 supports 10BASE5 thickwire and 10BASE2 ThinWire connections. The 10BASE2 connection requires an external transceiver.

When the AUI port is selected, the following AUI signals can be active:

Signal	Pin Number
AUI_RD–	110
AUI_RD+	109
AUI_TD–	101
AUI_TD+	100
AUI_CD–	107
AUI_CD+	106

When the 10BASE-T port is selected, the following twisted-pair signals can be active:

Signal	Pin Number
TP_RD–	105
TP_RD+	104
TP_TD+ +	97
TP_TD–	96
TP_TD+	95
TP_TD– –	94

These signals interface with the Manchester encoder/decoder portion of the 21041.

3 Physical Layer

The physical layer of the 21041 can be used in AUI or 10BASE-T configurations. Different methods are used to connect each port to the actual cable connector.

3.1 10BASE-T Twisted-Pair Network Port

Figure 1, Figure 2, and Figure 3 show the physical layer design options for 10BASE-T type implementations. Figure 1 and Figure 2 show two ways of connecting the 10BASE-T network by using a standard 1:1 transformer module. This implementation type requires a swing compensator (to swing the 21041 output from 3.3 V to 5.0 V) to meet the standard requirements. Figure 3 shows a direct connection to a 1: $\sqrt{2}$ transformer module. This implementation type provides the lowest component count for 10BASE-T. The filter and transformer components minimize any potential electromagnetic interference and radio frequency interface problems. Common-mode noise (when noise between two lines of the same polarity, add rather than cancel) can radiate energy from the twisted-pair interface. Also, significant common-mode power supply noise can be generated on the board or adapter by other devices. Therefore, Digital recommends the use of filter and transformer modules that incorporate common-mode chokes. Table 1 and Table 2 list the optional part numbers for each implementation.

Figure 1 shows the 10BASE-T network connection with buffers. The required components for this configuration are as follows:

- Voltage swing compensator—74ACT244
- Terminating and decoupling components
- Filter transformer and common-mode chokes
- RJ45 connector

Figure 1 10BASE-T Network Connection

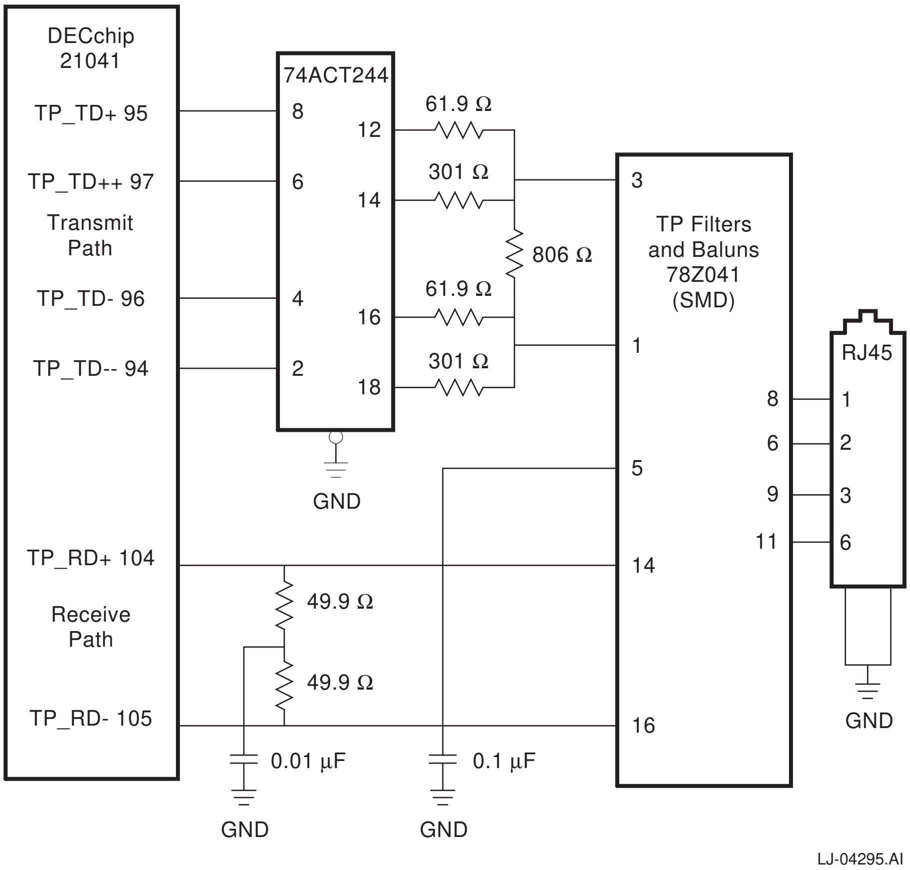

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Figure 2 shows the 10BASE-T network connection *without* buffers. The required components for this configuration are as follows:

- Terminating and decoupling components
- Transformer module (ratio of 1: $\sqrt{2}$ for swing compensation)
- Filter transformer and common-mode chokes
- RJ45 connector

Figure 2 10BASE-T Network Connection Without Buffers

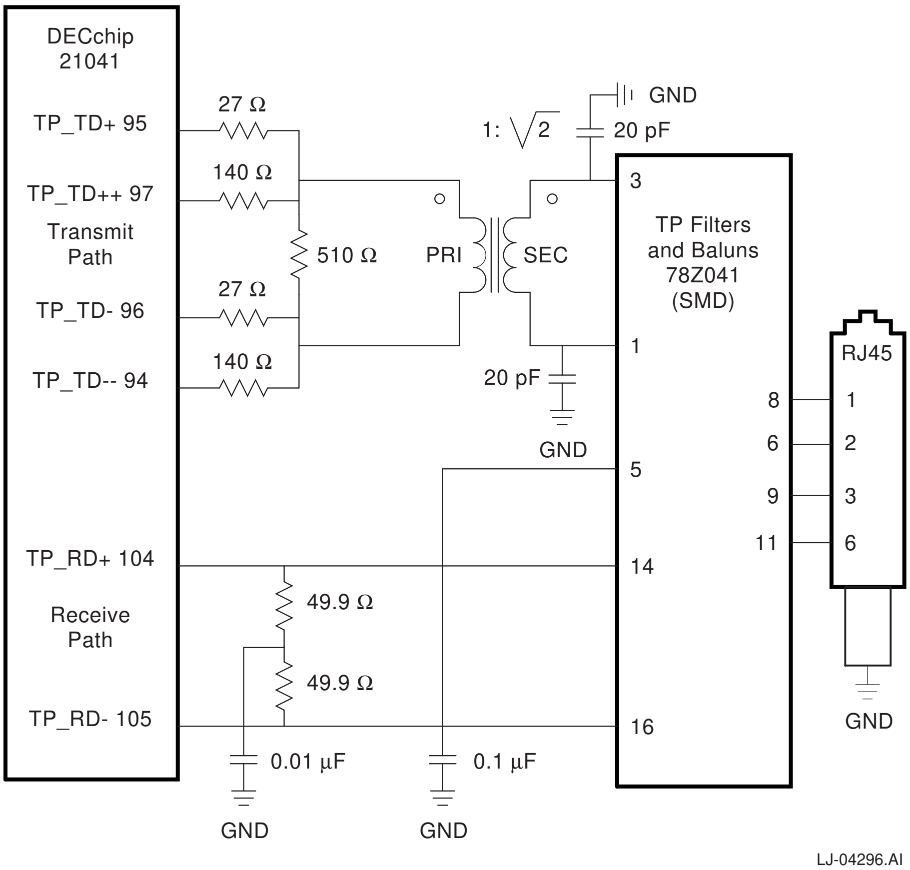
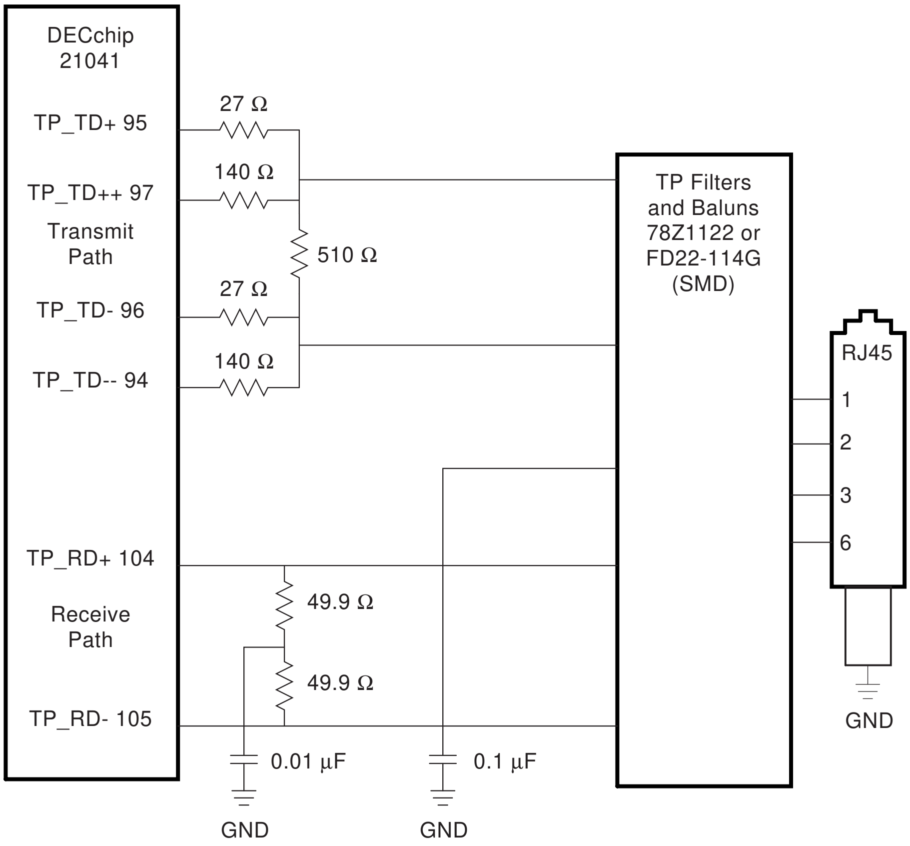


Figure 3 shows the minimum component requirement for the 10BASE-T network connection. This implementation uses a filter transformer module with a 1: $\sqrt{2}$ transformer on the transmit path to compensate for the voltage swing. The required components for this configuration are as follows:

- Terminating and decoupling components
- Filter, transformer, and common-mode chokes
- RJ45 connector

Figure 3 Minimum 10BASE-T Network Connection



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3.2 AUI Network Port

The 21041 is fully compliant with the AUI standard. The AUI can interface with an external medium-attachment unit and connect to alternate media, such as 10BASE2 (ThinWire) and 10BASE5 (thickwire). Figure 4, Figure 5, and Figure 6 show the required connections.

Figure 4 shows the AUI 10BASE5 network connection and the pin connections between the DECchip 21041 and the isolation transformer. The required components for this configuration are as follows:

- Terminating and decoupling components
- Isolation transformer
- AUI connector

Figure 4 AUI 10BASE5 Network Connection

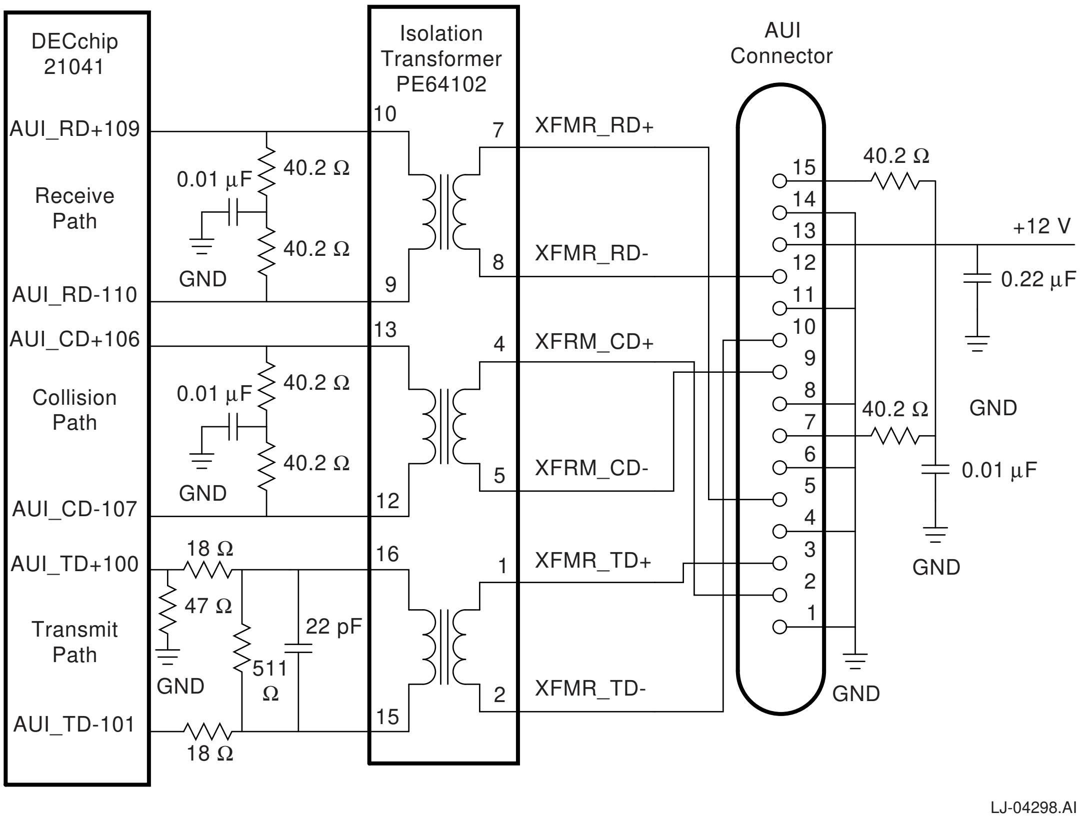
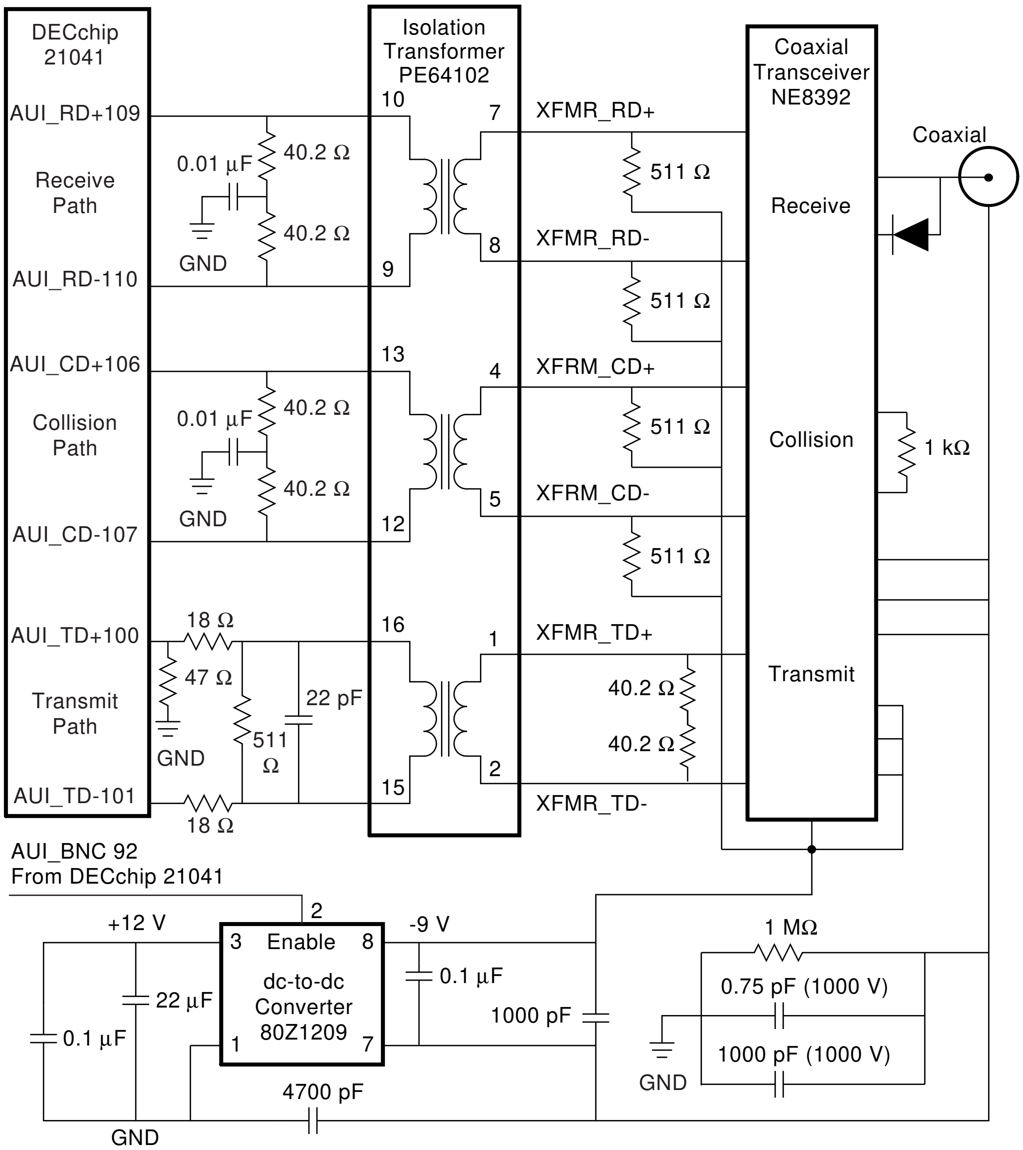


Figure 5 shows the AUI 10BASE2 network connection. In this configuration, the attachment unit interface (AUI) is not externally exposed. The required components for this configuration are as follows:

- Isolation transformer
- Terminating and decoupling components
- dc-to-dc converter
- Coaxial transceiver and BNC connector

Figure 5 AUI 10BASE2 Network Connection



Note:
Refer to the vendor data sheet for the specific implementation of the coaxial transceiver (NE8392).

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Implementing Network Connections

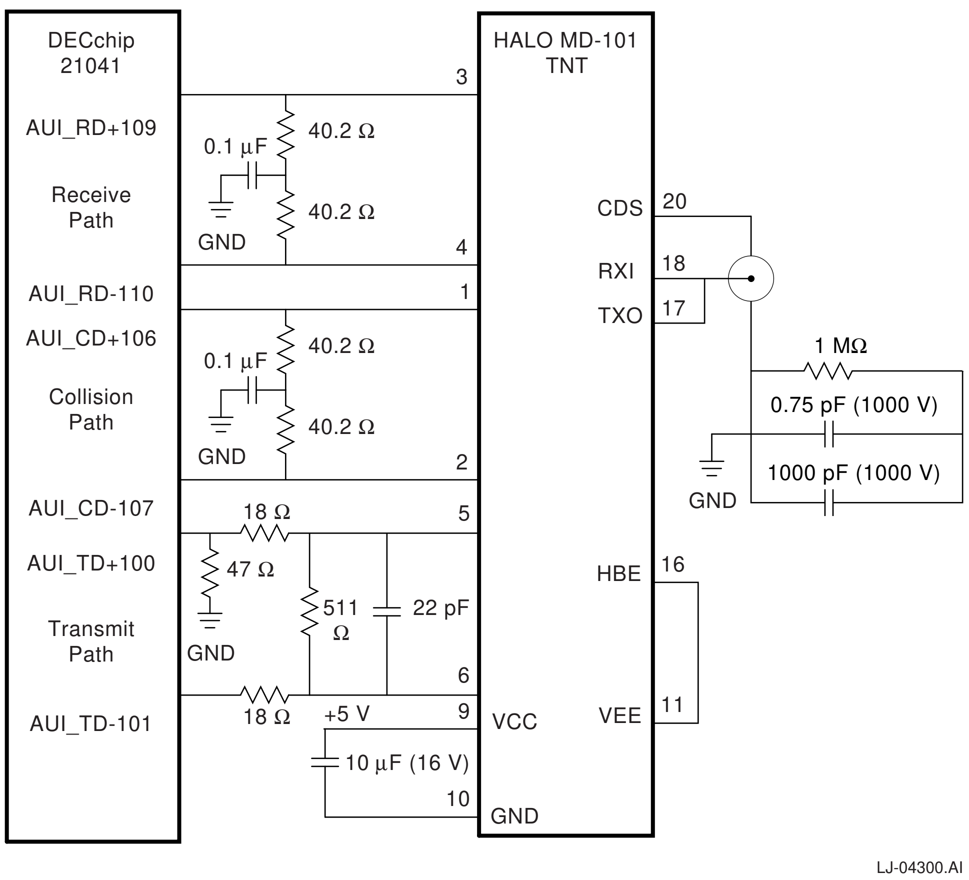
In cases where the 10BASE2 medium-attachment unit is a module separate from the board, the medium-attachment unit can be implemented on a small add-in card. Ensure that the cable used to connect the board to the medium-attachment unit provides adequate shielding of the attachment unit interface signals from external noise. This medium-attachment unit add-in card includes the following components:

- Transceiver chip and BNC connector
- dc-to-dc converter
- Discrete devices

Figure 6 shows the AUI 10BASE2 network connection with a Thin Net Transceiver (TNT). The required components for this configuration are as follows:

- Termination and decoupling components
- TNT transceiver
- BNC connector

Figure 6 AUI 10BASE2 Network Connection with Thin Net Transceiver (TNT)



3.3 Media-Specific Components

Table 1 lists the media-specific interface components for 10BASE-T access.

Table 2 lists the media-specific interface components for 10BASE2 and 10BASE5 access.

Table 1 10BASE-T Media-Specific Components

Access Type	Components	Available Part Numbers
10BASE-T	74ACT244 driver	74ACT244 or 74FCT244
	Filter and transformer module	Pulse Engineering PE65745 (SMD[1]), Valor PT4096 (SMD[1]), Valor ST7011 (SMD[1]), Halo TD42-2006Q (SMD[1]), or Halo TG42-2006W1 (SMD[1])
	Transformer filter and chokes	Pulse Engineering PE65434 or Valor FL1012
	RJ45 wire jack connector	—

[1]Surface mount device

Table 2 10BASE2 and 10BASE5 Media-Specific Components

Access Type	Components	Available Part Numbers
10BASE2	dc-to-dc converter	Filmag 80Z1209
	Isolation transformer	Pulse Engineering PE64102 (SMD[1]), Pulse Engineering PE65723(SMD[1]), Valor LT6032 (SMD[1]), Valor ST6032/3 (SMD[1]), Halo TD01-0756K (SMD[1]), or Halo TG01-0756W (SMD[1])
	Transceiver	National DP8392C
	Connector	—
10BASE5	Isolation transformer	Pulse Engineering PE64102 (SMD[1]), Pulse Engineering PE65723 (SMD[1]), Valor LT6032 (SMD[1]), Valor ST6032/3 (SMD[1]), Halo TD01-0756K (SMD[1]), or Halo TG01-0756W (SMD[1])
	AUI connector	—

[1]Surface mount device

3.4 Layout Considerations

The 21041 implements the function of the 10BASE-T transceiver, the AUI transceiver, and the full PCI bus connection on the chip.

The 21041 requires a minimum of external components to implement the network connection, however, when implementing the connection, you must adhere to the requirements for electromagnetic and radio frequency interference.

Figure 7 shows the 21041 external component connections.

Figure 7 21041 External Component Connections

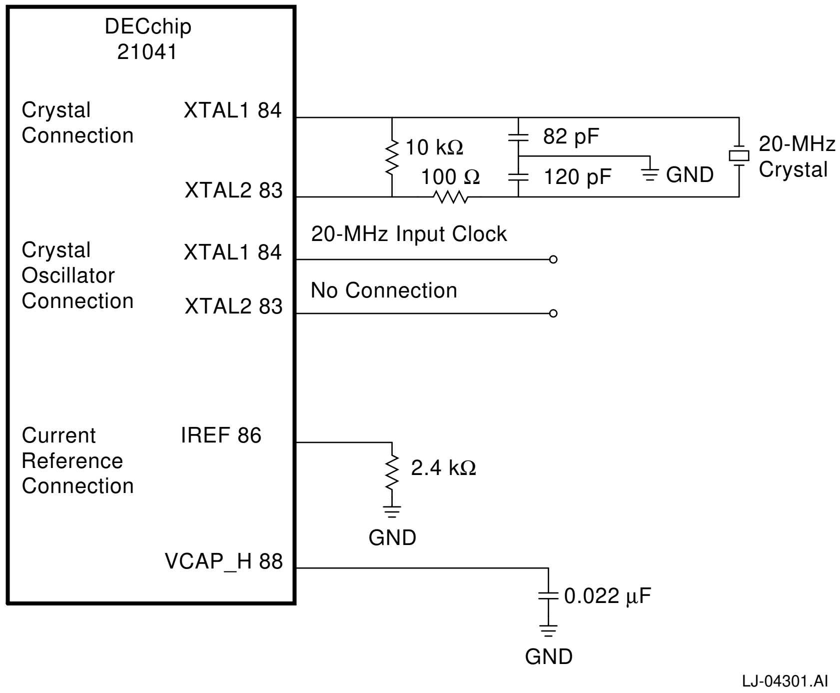


Table 3 lists the specifications for the crystal.

Table 3 Crystal Specifications

Specification	Value	Units
Crystal frequency	20.000	MHz
Frequency tolerance	±50	PPM
Load capacitance	50	pF
Frequency stability	±30	PPM
Maximum effective series resistance	40	Ω
Test condition drive level	100	µW

3.4.1 Signal Routing and Placement

The Ethernet circuitry should be kept free of interference from unrelated signal traces. Routing for other signals must be kept away from the space surrounding the grouped Ethernet components. Place the Ethernet circuitry at the perimeter of the board, as close as possible to the network connector.

The onchip crystal oscillator requires an external crystal and discrete components. For stable and noise-free operation, place the crystal and discrete components as close as possible to the 21041, keeping the etch length as short as possible. Do *not* route any noisy signals in this area.

The PCI pin ordering is fully compatible with the PCI specification recommendation for allowing easy routing of the PCI signals within the etch limits as specified. This includes shared signal lengths of up to 3.8 cm (1.5 in) and the clock signal length of 6.41 cm (2.5 in).

Keep all signal paths short and route them as directly as possible.

Systems using the 10BASE-T nodes can be connected by cables up to 100 m. As a result, the signal that reaches the board can be noisy and low in amplitude. To minimize corrupting this data, route these signals, by the most direct path, from the network connector to the 21041.

The length of this path should not exceed 8 cm (3 in) for the following receive data signals:

Signal	Pin Number
AUI_RD–	110
AUI_RD+	109
AUI_CD–	107
AUI_CD+	106
TP_RD–	105
TP_RD+	104

3.4.2 Ground and Power Planes

Up to four types of power signals require handling when implementing a design with the 21041:

- **GND** is adapter ground.
- **VCC** (+5 V from PCI) drives the external components (boot ROM and Ethernet address ROM).
- **VDD** (+3.3 V) drives the 21041.
- **VEE** (–9.0 V) powers the dc-to-dc converter if the coaxial network connection is implemented. For the specific –9 V power supply, refer to the transceiver used to drive the coaxial network connection.

Digital recommends that at least two power planes be kept on the PCB: **VCC** and **GND**. The **VDD** power plane (3.3 V) can be implemented either by a cut in the **VCC** power plane or by a power island under the 21041 on one of the signal routing layers.

Digital recommends decoupling capacitors should be added for all power supplies. These capacitors should be placed as close as possible to the power pads of the chips. The recommended values are as follows: 0.1 µF, 0.01 µF, 10 µF (tantalum), and 47 µF (tantalum).

For better noise testing immunity, remove all power planes between the network connectors and the transformer on both the 10BASE-T and 10BASE2 connections.

Digital also recommends that the connector’s shield of the adapter should be connected to the PC chasis.

3.4.3 3.3-V Power Supply

The 21041 operates with a power supply of 3.3 V. At least eight decoupling capacitors are recommended and should contain the following values:

- Two each at 0.1 µF
- Two each at 0.01 µF
- Two each at 10 µF (tantalum)
- Two each at 47 µF (tantalum)

3.4.4 Crystal and Crystal Oscillator Connections

Figure 7 shows two serial clock connections; select either the crystal connection or crystal oscillator connection.

According to the IEEE 803.2 standard, a 20-MHz crystal is required. The crystal frequency must not vary by more than 100 parts per million (PPM), or 0.01 %. Place the crystal as close as possible to the 21041.

Because the frequency of crystals from different vendors can vary, test the crystals in the actual circuit. It may be necessary to vary the tuning of the surrounding components. However, after the capacitors have been tuned for the specific crystal, the design does not need to be altered on a board-by-board basis.

The 21041 also supports a crystal oscillator (Figure 7). In this configuration, no external component is required and the **XTAL2** pin should be left open. This is useful for applications with multiple network connections.

3.4.5 LED Status Signals

The LED connection requires a serial resistor that is connected to ground. This resistor value should be calculated according to the type of LED used. A typical 2-mA LED requires a 750-Ω resistor. For implementations using the boot ROM, the LED current should not exceed 2 mA. Table 4 lists the seven LED status signals.

Table 4 LED Status Signals

LED	Description	Pin Number
Transmit	Indicates a transmit operation is in progress.	113
Collision	Indicates that the 21041 detected a collision on the network.	114
Receive match	Indicates a received packet is identified by the 21041 as the packet addressed to this station.	115
Receive	Indicates a receive operation is in progress.	116
Polarity	Indicates correct polarity on the twisted-pair receive lines.	117
Transmit jabber	Indicates that the 21041 is in transmit jabber state.	118
LINK_PASS	Indicates that a link is established in TP operating mode.	119

3.4.6 Other Considerations

The current reference input (IREF, pin 86) for the analog-phase-locked loop (PLL) should be connected through a 2.4-k Ω resistor to ground. The capacitor input (VCAP_H, pin 88) should be connected through a 0.022-µF capacitor to ground (Figure 7).

If the JTAG port is unused, leave the following JTAG pins open: TMS (pin 1), TDI (pin 2), and TDO (pin 4). The 21041 internally pulls the TDI and TMS pins up. If the JTAG port is not used, TCK (pin 120) must be pulled up or down.

Technical Support and Ordering Information

Technical Support

If you need technical support or help deciding which literature best meets your needs, call the Digital Semiconductor Information Line:

United States and Canada	**1–800–332–2717**
TTY (United States only)	**1–800–332–2515**
Outside North America	**+1–508–568–6868**

Ordering Digital Semiconductor Products

To order the DECchip 21041 PCI Ethernet LAN Controller and Evaluation Board, contact your local distributor.

You can order the following semiconductor products from Digital:

Product	Order Number
DECchip 21041 PCI Ethernet LAN Controller	21041–AA
DECchip 21041 Evaluation Board Kit	21A41–01
DECchip 21040 Ethernet LAN Controller for PCI	21040–AA
DECchip 21040 Evaluation Board Kit	21A40–01
DECchip 21140 PCI Fast Ethernet LAN Controller	21140–AA
DECchip 21140 Evaluation Board Kit	21A40–03

Ordering Associated Literature

The following table lists some of the available Digital Semiconductor literature. For a complete list, contact the Digital Semiconductor Information Line.

Title	Order Number
DECchip 21041 PCI Ethernet LAN Controller Product Brief	EC–QAWVA–TE
DECchip 21041 PCI Ethernet LAN Controller Data Sheet	EC–QAWWA–TE
DECchip 21041 PCI Ethernet LAN Controller Hardware Reference Manual	EC–QAWXA–TE

Ordering Third-Party Literature

You can order the following third-party literature directly from the vendor:

Title	Vendor
PCI Local Bus Specification, Revision 2.0	PCI Special Interest Group N/S HH3–15A 5200 N.E. Elam Young Pkwy Hillsboro, OR 97124–6497 1–503–696–2000
Institute of Electrical and Electronics Engineers (IEEE) 802.3	IEEE Service Center 445 Hoes Lane P.O. Box 1331 Piscataway, NJ 08855–1331 1–800–678–IEEE (U.S. and Canada) 908–562–3805 (Outside U.S. and Canada)