Digital Semiconductor

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DECchip 21130 PCI Integrated Graphics and Video Accelerator Evaluation Board Design Example:

An Application Note

Order Number: EC–QHV4B–TE

July 1995

This application note describes the DECchip 21130 evaluation board (EB130) design. PCI graphics designers and manufacturers can use this note when designing with the DECchip 21130 PCI Integrated Graphics and Video Accelerator chip.

Revision/Update Information: This document supersedes the *DECchip 21130 PCI Integrated Graphics and Video Accelerator Evaluation Board Design Example: An Application Note* (EC–QHV4A–TE).

Operating System and Version: Any IBM PC compatible system

Digital Equipment Corporation
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While Digital believes the information included in this document is correct as of the date of publication, it is subject to change without notice.

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Introduction to the EB130

The DECchip 21130 PCI Integrated Graphics and Video Accelerator Evaluation Board (EB130) is intended to serve both as a design example for customer evaluation and software development, and as a low-cost, ready-to-manufacture design.

EB130 Features

The EB130 has the following features:

- 64-bit 264MB/s frame buffer interface
- Integrated digital-to-analog converter (DAC) and color lookup RAM
- Integrated video playback pipeline
- Integrated pixel clock phase-locked loop (PLL)
- Integrated memory clock PLL
- Supports 1MB, 2MB, and 4MB extended data-out (EDO) DRAM and DRAM frame buffers
- Direct memory access (DMA) for high bandwidth video pipeline
- 64K × 8 BIOS flash ROM
- Compliance with *PCI Local Bus Specification Revision 2.0*
- VESA standard VGA pass-through connector
- VESA DDC1 and DDC2 monitor communication protocol
- VESA Display Power Management System (DPMS) support
- Standard 15-pin VGA video connector
- Low-cost, 4-layer printed circuit board
- Reduced PCI *short card* profile
- FCC- and CE-tested design

EB130 Design

DECchip 21130 Design Choices

The DECchip 21130 is a highly integrated chip that requires a minimum of external components. Most design choices are based on the total amount and type of DRAM required and the physical topology required. Timing analysis is, in general, not required as long as DRAMs that have been qualified by Digital Semiconductor are used and layout rules described in this note are followed. The DRAM choices and DRAM application notes are covered in a separate document, the *DECchip 21130 PCI Integrated Graphics and Video Accelerator Compatible Memory Devices: An Application Note.*

Design Requirements

The EB130 design choices were based on the following requirements dictated by our customers.

- Ready-to-manufacture design for fast product launch
- Low-cost, minimum profile printed circuit board
- Maximum of 4MB frame buffer memory
- 64KB BIOS flash ROM
- VESA VGA pass-through connector
- FCC- and CE- tested design

EB130 Physical Description

The EB130 is implemented on a 4-layer printed circuit board that measures 4.2 in × 5.8 in. All active components are surface mounted on the top side of the board (side B as defined in the PCI specification). All passive parts except for the 15-pin video connector and 26-pin VGA pass-through connector are surface mount types. Most of the passive components are mounted on the bottom side of the board (side A as defined in the PCI specification). The bottom side mounting of decoupling capacitors and some resistors allows for their optimal placement as well as cleaner routing of the 4-layer printed circuit board.

The first 2MB of EDO DRAMs are soldered directly to the board, while the second 2MB are socketed to allow customer field upgrades. A 1MB version of the board is possible by de-populating two of the four EDO DRAMs in the first bank. The drivers supplied with the EB130 will automatically detect the amount of DRAM installed on the board.

An industry-standard, 15-pin D-sub video connector is mounted in the lower left corner of the board.

An industry-standard, 26-pin VGA pass-through connector is mounted in the upper right corner of the board.

A 64K × 8 flash ROM is soldered to the board and can be programmed in circuit by software provided with the EB130.

Primary Components

The following sections describe the primary components of the EB130.

DECchip 21130

The DECchip 21130 is a 208-pin plastic quad flat pack (PQFP) semicustom chip that interfaces directly to the industry-standard 32-bit PCI local bus; industry-standard EDO DRAMs on a 64-bit frame buffer bus; and industry-standard flash ROM. Integrated pixel clock and memory clock PLLs and video DAC require one external crystal and one voltage reference part. Glue logic is not required to implement a minimum system.

EDO DRAM

The 21130 is designed to perform best with extended data-out, dynamic random-access memory (EDO DRAM). The EDO feature allows the EDO DRAM to latch and hold the read data on the rising edge of the CAS strobe. Non-EDO DRAMs tristate their data drivers when CAS is high, requiring the memory controller to latch the data while CAS is low. This EDO function allows the data hold time to be overlapped with the CAS precharge time of the next cycle. This results in shorter page mode cycle times and higher read bandwidth.

Note

DECchip 21130 operation with standard DRAMs (non-EDO) is also possible. Refer to the *DECchip 21130 PCI Integrated Graphics and Video Accelerator Compatible Memory Devices: An Application Note* for details about qualified EDO DRAMs, and DRAMs.

Flash ROM

The 21130 directly interfaces with up to 256KB of industry-standard flash ROM. A 64KB part is used in the EB130, as this is the minimum required to store the EB130 BIOS codes.

14.31818-MHz Crystal

The pixel clock and memory clock PLLs integrated into the 21130 require an external crystal frequency reference. An internal oscillator circuit drives the 14.31818-MHz crystal.

1.2-V Voltage Reference

An accurate 1.2-V voltage reference is required for the integrated DAC in the 21130.

Component Substitutions

All components with the exception of the DRAM may be substituted with suitable types. Refer to the *DECchip 21130 PCI Integrated Graphics and Video Accelerator Compatible Memory Devices: An Application Note* for details about qualified EDO DRAMs. Industry standard flash ROMs that conform to 28F512 write timing and protocol may also be used. Industry-standard 150-ns ROM may also be used if flash writing is not required.

EB130 Board Revisions

There are two revisions of the EB130. Etch Revision A only supports 21130 chip Revisions B and C, while etch Revision B supports 21130 chip Revisions B, C, and E.

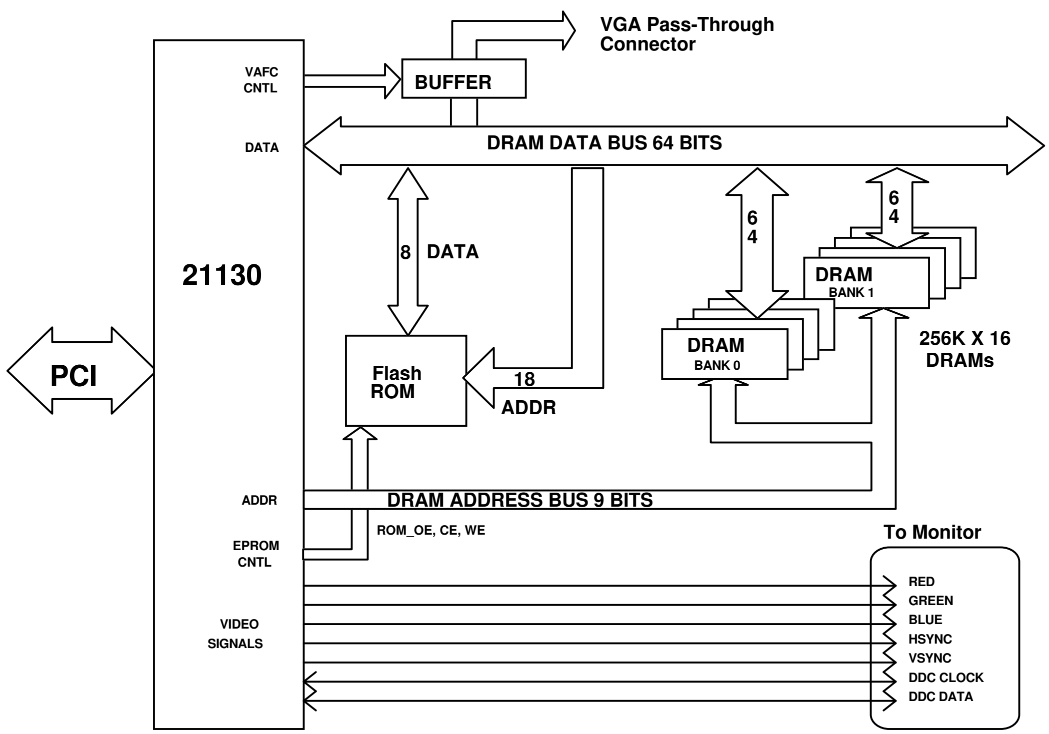
The following is a list of changes to EB130 etch Revision A that are incorporated in etch Revision B:

1. Add third **Vdd** filter network to power 21130 pin 41.
2. Modify **Vdd** filter networks to include a 10-Ω series resistor.
3. Add two 15-kΩ resistors (R26 and R27) to pull-up DDC_SDA and DDC_SCL signals.
4. Connect PWRP12 (positive 12 V) signal to R4 to allow writing flash ROM.
5. Move E5 and C1 to allow socket on DRAM E1.

EB130 Circuit Schematic Design Description

The following section describes design details shown in the EB130 schematics. Refer to the EB130 schematics supplied with the EB130 kit and the EB130 block diagram shown in Figure 1 while reading this application note.

Figure 1: EB130 Block Diagram



Sheet 2

Sheet 2 of the schematics shows the 14.31818-MHz crystal used as the frequency reference for the pixel clock and memory clock PLLs integrated into the 21130 chip. The capacitors connected to the crystal are not required for 21130 Revision B or C and are not mounted on the board. Installing these capacitors with 21130 Revision B or C may result in unstable PLL operation. Capacitors internal to the 21130 Revisions B and C on the XTAL1 and XTAL2 pins perform the required filtering. The crystal is mounted close to the XTAL1 and XTAL2 pins on the 21130. For 21130 Revision E, 10-pF capacitors must be mounted in C30 and C32 positions.

The PCI finger block shows the finger numbers and signal names assigned to the standard PCI signals. Note that the A fingers are on the bottom side of the board and the B fingers are on the top (component) side of the board. The two PCI PRSNT signals are tied to ground on the board to signal the host that this board consumes less than 7.5 W of power.

The signals GP_CS# and GP_STB# have configuration resistors R20, R21, R22, and R24 that are used to force the 21130 to use its internal PLLs as the source of pixel clock and memory clock and to use its internal video timing generator to drive the horizontal sync, vertical sync, and blanking signals. Resistors R20 and R24 that connect these signals to ground are not mounted on the board and resistors R21 and R22 that connect these signals to **Vcc** are mounted. Installing resistors R20 and R24 will not allow the 21130 to function. These configuration options, intended for engineering evaluation of the 21130, are not required in a finished product.

Sheet 3

Sheet 3 of the schematics shows the 21130 and some of the passive components required to support it. The symbol for the 21130 is organized to group the primary buses and functions together.

The PCI Interface section on the left of the symbol connects directly to the PCI fingers with the exception of the PCI_CLK signal, which has a series 10-Ω resistor, R19. This resistor is used for engineering tests of PCI clock skews and could be replaced by a 0-Ω resistor or eliminated in a new design.

The lower section of the 21130 symbol shows all of the digital power and ground pins used by the 21130. These pins are connected directly to the **Vcc** and GND layers.

The frame buffer interface is shown on the right of the 21130 symbol. All signals are wired directly to the DRAM array except for RAS2#, which is not connected in this 4MB design.

The GPP signal group is shown in the top right of the 21130 symbol. These signals are used to control the flash ROM on the EB130. GP_STB# connects to the flash ROM OE# pin, and ROM_CE# connects to the flash ROM CE# pin. GP_INT# is pulled up to **Vcc** and is not used in the EB130 design. GP_CS# and GP_RESET are also not used in the EB130 design.

The top left section of the 21130 symbol shows the VAFC interface that contains the signals necessary to control the VESA VGA pass-through connector supported in the EB130 design. This section also has the monitor timing signals DC_VSYNC, DC_HSYNC, and DC_BLANK#. The DC_ prefix indicates that these signals are directly connected to the 21130 chip. The VGAFC_DATA_2, VGAFC_DATA_1, and VGAFC_DATA_0 signals are the lower 3 bits of the VGA pass-through connector data bus (note that the upper 5 bits are derived from the BMEMDATA_<63:59> signal).

The middle left section of the 21130 symbol contains the DAC and PLL functions. This section has dedicated **Vdd** and **Vss** pins for the DAC and PLL. Power for the DAC and PLL **Vdd** pins is derived from the main 5-V **Vcc** power layer through ferrite filters, resistors and decoupling capacitors. Dedicated DAC and PLL **Vss** are connected directly to the ground layer of the board. Special treatment of the power and ground layers is discussed later in this note.

Sheet 4

Sheet 4 of the schematics shows the lower 2MB bank of frame buffer memory. Each byte in the 64-bit frame buffer data bus has a DRAM_CAS# signal associated with it. The eight DRAM_CAS<7:0> signals provide byte-level write control across the 64-bit frame buffer data bus. DRAM_RAS1# is connected to the bank 0 DRAM that is connected to frame buffer data bits 16 through 31 while the rest of the DRAMs in bank 0 are connected to DRAM_RAS1#. The use of DRAM_RAS1# in this manner provides access control for the VGA functions built into the 21130.

Sheet 5

Sheet 5 of the schematics shows the upper 2MB bank of frame buffer memory. All DRAMs in this bank are connected to DRAM_RAS2#. The double diode devices on this sheet are active termination for the DRAM control lines. Active termination provides the best possible signal settling times without introducing additional delays. The diodes trim undershoot on the signals by clamping them to ground. In addition, the diodes used have a low forward breakdown voltage, which serves to trim overshoot. Some of these diodes may be deleted to reduce cost if it is determined that the signals do not require active termination. Any suitable fast signal clamping diode may be used for active signal termination.

Sheet 6

Sheet 6 shows the VGA feature connector (FC) and buffer as well as the flash ROM. The 74F245 octal transceiver is used to buffer BMEMDATA<63:59> and VGAFC_DATA<2:0> to the feature connector. When the VGA mode is active, the upper 5 bits of the frame buffer data bus BMEMDATA<63:59> are redefined to supply pixel data to the VGA feature connector. The lower 3 bits of the FC are supplied by dedicated 21130 pins VGA_DATA<2:0>. The control signals EVIDEO#, ESYNC#, and EDCLK# are driven by whatever device may be connected to the VGA FC. The signals DC_VAFC_DCLK, DC_BLANK#, DC_HSYNC, and DC_VSYNC are driven directly by the 21130 and are series damped before driving the VGA FC. The series damping provides overshoot control and also serves to reduce possible electromagnetic interference (EMI). The VAFCDATA_<07:00> lines from the 74F245 have 56-pF capacitors connected to them to remove high frequency components that may cause EMI problems. The values of the series dampers and capacitors may be adjusted to improve EMI performance.

The flash ROM uses BMEMDATA<49:32> as address lines A<17:0> during ROM access cycles. BMEMDATA_58 provides the ROM WE# function, and BMEMDATA<57:50> provides the ROM read and write data. The flash ROM VPP program potential pin is incorrectly shown connected to **Vcc** on etch Revision A boards; it should be connected to 12 V. An etch cut and wire on the EB130 etch Revision A corrects this error. Etch Revision B also corrects this error. The series resistor R4 is provided to allow write-protecting the flash ROM by deleting the resistor from the parts list.

Sheet 7

Sheet 7 shows the 15-pin D-sub video connector; its associated static protection diodes; EMI filter capacitors and resistors; and the RED, GREEN, and BLUE analog video termination resistors. The static protection diodes and not critical and can be of any suitable type. Also on this sheet is the filtered and decoupled PWR_DAC_5 power feed to the DAC_VDD pins on the 21130. The 1.2-V voltage reference device that supplies VREF to the DAC and FSADJ resistor, R14, is located close to the respective pins on the 21130.

Pin 15 on the 15-pin D-sub video connector is labeled DDC_SCL and is connected by a series damping resistors to the PLL_TEST signal on the 21130. The PLL_TEST signal is a dual-purpose signal that normally functions as the DDC_SCL function. The diagnostics provided with the EB130 can be used to redefine this pin to be a test point that provides either the pixel clock or memory clock from the internal PLLs. System RESET will initialize this signal to its DDC_SCL function. Etch Revision A required the deletion of static protection diodes D1 and D4 in order to mount 15-kΩ pull-ups on the DDC_SDA and DDC_SCL signals. Etch Revision B adds 15-kΩ resistors R26 and R27 to correct this omission.

Sheet 8

Sheet 8 shows a cap farm of bulk tantalum and ceramic capacitors used to decouple the 5-V and 12-V power rails. The ceramic capacitors are mounted on the bottom side of the board as close as possible to each DRAM and power pin on the 21130.

21130 Revision E Support

The EB130 etch Revision B supports 21130 chip Revisions B, C, and E. DECchip 21130 Revisions B and C require that capacitors C30 and C32 on signals XTAL1 and XTAL2 not be installed and that resistor R14 on signal FSADJ be 150 Ω.

DECchip 21130 Revision E requires that capacitors C30 and C32 on signals XTAL1 and XTAL2 be 10 pF and that Resistor R14 on signal FSADJ be 374 Ω (see Table 1).

Table 1: Capacitor and Resistor Requirements

Capacitor/Resistor	Chip Revision	
	B, C	E
C30, C32	None	10 pF
R14	150 Ω	374 Ω

Electromagnetic Interference Management

EMI management in the EB130 design consists of the following four strategies:

- Reduction of high frequency components in the analog video signals
- Isolation of power and ground regions in the video connector and I/O bulkhead section of the board
- Careful routing of critical signals and placement of critical components
- Filtering of the DAC power pins

High Frequency Reduction

The three digital-to-analog converters (DACs) integrated into the 21130 are of the constant current type. This DAC type will source a constant current relative to the digital input value. Constant current DACs can source current into a termination resistor or ground. Constant current DACs are linear within a specified compliance voltage range, generally under 2 V. Due to this constant current design, unwanted high frequency components in the DAC outputs are best shunted to ground through a capacitor. This method of high frequency roll-off is better suited to constant current DACs than high frequency ferrites or chokes. The EB130 places a 56-pF capacitor close to each video output pin in the 15-pin D-sub connector. The value of this capacitor was chosen as a trade-off between adequate EMI margin and the desire for good rise and fall times on the video signals. New designs based on the 21130 may need to adjust the value of this capacitor to meet EMI agency requirements.

Power and Ground Isolation

Holding the EB130 board up to a light source will reveal the channels cut into the power and ground layers between the RED, GREEN, and BLUE pins on the 21130 and the video connector and I/O bulkhead.

Figure 2 shows the channels that are cut into the ground layer. Note that there is a small area between the two channels that connects the analog ground to the digital ground. This split forces digital and analog return currents to keep to their respective areas and also serves to isolate the digital ground noise from the I/O bulkhead.

Figure 2: Analog and Bulkhead Ground Layer Split

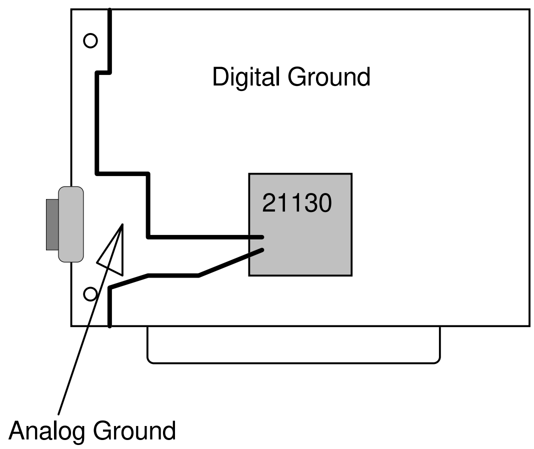
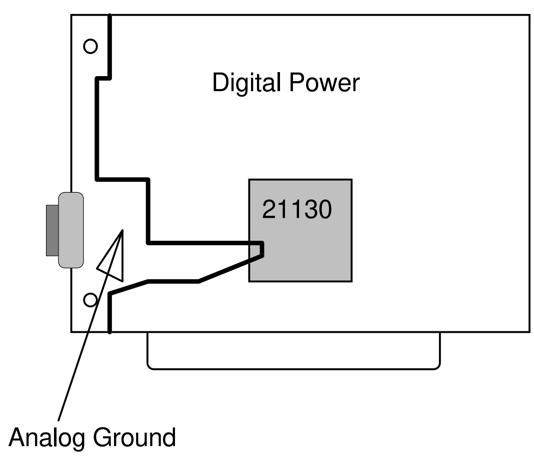


Figure 3 shows the channels that are cut into the power layer. Note that the power layer is completely isolated from the I/O area. The isolated island is tied to the analog ground area through the several ground vias that are in this area. The I/O bulkhead screw holes, vias, and pads are also tied to the analog ground island.

Figure 3 : Analog and Bulkhead Power Layer Split



Signal Routing and Component Placement

Careful attention is paid to ensure that no signal traces cross the isolation splits. Failure to ensure this will result in increased loop area for any signals that cross the split and increased electromagnetic radiation from these signals. All signals in the analog island are routed as short and direct as possible with the fewest possible vias.

The components associated with the DAC are placed as close as possible to the pins they connect to on the 21130. The capacitors connected to the RED, GREEN, and BLUE signals are located as close as possible to the video connector. Each capacitor is tied to ground through a via located close to the capacitor pad. Daisy chaining of ground signals should be avoided.

DAC Power Filtering

The 21130 Revisions B and C have two power pins dedicated to the DAC while 21130 Revision E has only one. The power supply to these pins is isolated from the main digital 5-V supply via two filter networks that consist of a ferrite bead, resistor, and decoupling capacitors. The ferrite beads are surface mount types that straddle the inner layer power and ground spilt. The resistors and decoupling capacitors are placed inside the analog isolation island, and the PWR_DAC_5 and PWR_5A (**Vdd**) connections are routed as normal signal traces to 21130 power pins 41 and 42, the decoupling capacitors, and the ferrite bead. The capacitors are placed as close as possible to the 21130 power pins. This scheme reduces the coupling of unwanted digital noise into the DAC and provides a clean power supply to the DAC without the need for a separate regulator.

Note

The B and C revisions of the 21130 require one filtered **Vdd** source for DAC **Vdd** pins, 41 and 42. The E revision of the 21130 chip uses pin 41 as a second PLL **Vdd** pin. This conflict requires adding a third **Vdd** filter network to supply power to pin 41. This allows pin 41 to function as a DAC **Vdd** for Revisions B or C and as a PLL **Vdd** pin for Revision E. New board designs should include two filtered power supply networks for pins 41 and 42. This will provide compatibility with all revisions of the 21130.

Backward Compatibility

To maintain board-level pin compatibility on different die steps of the 21130, two separate **Vdd** power filters are needed to supply 5-V to pins 41 and 42 on the 21130. The first release revision of the EB130 has only one filter for pins 41 and 42. The filter circuit, consisting of L2, R31, C34, C16, and C32 (as seen on sheet 7 of the schematics) must be duplicated to supply a separately filtered 5-V source to pin 42. Boards designs such as EB130 etch Revision B with separate filters for pins 41 and 42 will work with all die steps of the 21130.

Phase-Locked Loops

The 21130 has two phase-locked loops (PLLs) integrated into it: one for pixel clocks and one for memory clocks. Both of these PLLs use a common reference frequency of 14.31818 MHz, which is provided by an external crystal driven directly by the 21130 XTAL1 and XTAL2 pins. Parallel resonant type crystals are recommended.

PLL External Components

The PLLs require one external 14.31318-MHz crystal, and one external compensation capacitor. The capacitors C15 and C36 that are connected to the COMP pin on the 21130 are **not** part of the PLL low pass filter that is contained entirely within the 21130. The COMP capacitors are connected between the COMP pin and the PWR_PLL_5 pin and provide decoupling for internal analog circuits. Although two COMP capacitors are provided, only one is necessary. The additional COMP capacitor and its footprint are provided to allow for tuning of the compensation function if required.

The schematics show two 10-pF capacitors, C30 and C32, connecting the crystal XTAL1 and XTAL2 pins to ground. These two parts are not mounted when 21130 chip Revision B or C is used.

Power and Ground Isolation

Holding the EB130 board up to a light source will reveal the channels cut into the power and ground layers around the PLL power decoupling capacitors and crystal. The crystal is housed in a plastic 4-lead surface mount device with the two top-most leads providing mechanical support only and having no internal connection. Only the bottom two crystal leads are within the PLL analog ground region.

Figure 4 shows the channels that are cut into the ground layer. Note that there is a small area between the channels that connects the PLL analog ground to the digital ground. This split forces digital and PLL analog return currents to keep to their respective areas and also serves to isolate the digital ground noise from the PLL analog ground while maintaining a direct connection between digital ground and PLL analog ground.

Figure 4: Phase-Locked Loop Ground Layer Split

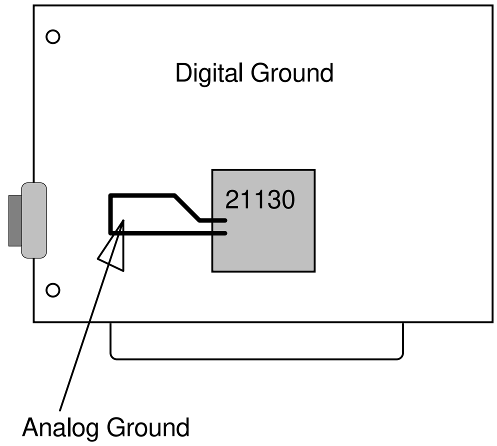
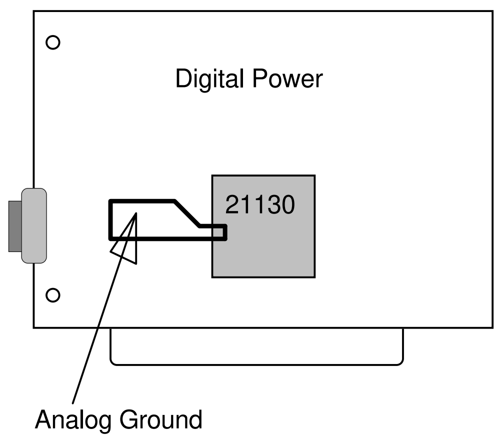


Figure 5 shows the split in the power layer of the 4-layer board. This split totally isolates the PLL island. The isolated island is connected to the PLL analog ground region by ground vias in the island. This scheme removes the digital power noise from the PLL analog island and improves PLL jitter performance.

Figure 5: Phase-Locked Loop Power Layer Split



PLL Power Filtering

The 21130 chip Revisions B and C have one power pin (pin 34) dedicated to the PLL, while Revision E has two PLL power pins (pin 34 and 41). The power supply to these pins is isolated from the main digital 5-V supply via a ferrite bead, resistor, and decoupling capacitors. The ferrite bead is a surface mount type that straddles the inner layer power and ground spilt. The resistor and decoupling capacitors for pin 34 are placed inside the PLL analog isolation island and the PWR_PLL_5 connections are routed as normal width signal traces to the 21130 PLL power pin, the resistor, decoupling capacitors, and the ferrite bead. The resistor and decoupling capacitors for pin 41 are placed inside the DAC analog isolation island and the PWR_PLL_5 connections are routed as normal width signal traces to the 21130 PLL power pin, the resistor, decoupling capacitors, and the ferrite bead. The PLL power capacitors are placed as close as possible to the 21130 PLL power pins. Because pin 41 is a DAC power pin in 21130 chip Revisions B and C and a PLL power pin in Revision E, the power filter components must be in one island or the other. Adding a third isolated island for the shared DAC/PLL power filter was not considered reasonable in the EB130 layout. The capacitors for pin 41, C60, C61, and C62 are mounted close to pin 41 and close to the ground peninsula that connects to the main **Vcc** layer to minimize DAC to PLL noise coupling. This scheme reduces the coupling of unwanted digital noise into the PLL and provides a clean power supply to the PLL without the need for a separate regulator. This scheme also serves to prevent high frequency PLL signals from coupling into the digital power and ground system and possibly causing EMI problems.

DECchip 21130 Power and Signal Connections

DECchip 21130 Power and Ground Connections

The 21130 has 15 power pins labeled VDD on the 21130 symbol that must be connected to the 5-V power layer (**Vcc**), and 18 ground pins labeled VSS that must be connected to the ground layer. Each VDD pin should have a 0.1-µF chip capacitor mounted as close as possible to the VDD pin. The ground pads of the 0.1-µF capacitors should be connected as close as possible to a ground via. Sharing of ground vias should be avoided. If ground vias must be shared, the connections should be made individually from the capacitors to the vias; daisy chaining of the ground connections will reduce system noise margins. Mounting the 0.1-µF decoupling capacitors on the back side (side A in the PCI specification) of the board is recommended because this results in the closest placement of the capacitors to the VDD pins.

The decoupling capacitors dedicated to the 21130 on the EB130 board are specially routed to allow easy isolation of the capacitor to 5-V layer connection as an aid to measurement of VDD current. This special treatment would not be required on new designs.

DECchip 21130 Signal Connections

All signal connections should be routed as short as possible. Special attention must be paid to the connections to the PCI fingers to assure that the signal trace length does not exceed the 1.5-in limit specified in the PCI specification.

Frame Buffer Signals

The EB130 uses termination diodes on all DRAM signals. These diodes clamp the signal lines and effectively reduce undershoot and overshoot. This improves signal settling times and reduces the possibility of ringing, which may cause false edges on the edge-sensitive RAS and CAS lines. The diodes should be placed as close as possible to the DRAM end of the signal trace. The DRAM address lines on the EB130 are routed to a point equidistant between the two blocks of DRAMs and are then routed as daisy chained stubs to the two DRAM blocks. This is intended to make the DRAM address lines approximate a lumped capacitive load and minimize transmission line effects. The use of series damping resistors instead of termination diodes will increase edge rates and may require reducing the memory clock frequency.

Video Signals

The RED, GREEN, and BLUE signal traces are routed on the back side of the board with minimal use of vias and the shortest possible trace length. These signals should be routed away from other signals in the analog I/O region. The 75-Ω termination resistors R11, R5, and R10 should be as close as possible to the 21130 pins. The EMI capacitors C21, C22, and C23 should be as close as possible to the pins on the 15-pin D-sub connector on the back side of the board. The static protection diodes D5, D6, and D7 can be mounted wherever is convenient as long as they do not increase the signal trace length.

The four digital signals that connect to the 15-pin D-sub have 75-Ω series damping resistors and 56-pF EMI capacitors. The EMI capacitors should be as close to the 15-pin D-sub as possible. The static protection diodes D1–D4 can be mounted wherever it is convenient.

Signal traces must not be allowed to cross the inner layer isolation splits. All signals should be at lease 0.02 in from the splits in the analog isolation island. The only exception to this is the **Vcc** signal trace that must be connected to the static protection diodes.

DDC Signals

The 21130 directly supports the VESA display data channel standard. Pin 30, DDC_IN, and pin 29, PLL_TEST, function as DDC_SDA and DDC_SCL, respectively. These signals are open collector and bidirectional. The PLL_TEST pin is a dual-function pin. After a system reset, it functions as DDC_SCL. The 21130 can be programmed to drive the internal PLL clocks out to this pin for engineering evaluation. This PLL test mode will cause very high frequency clocks to be driven on the monitor cable and will cause extreme EMI problems. The PLL test mode should never be used in a product; it is for engineering use only.

The DDC specification requires 15-kΩ pull-up resistors on the DDC_SCL and DDC_SDA signals on the video board. These resistors are missing in the original EB130 design. The resistors are added to the EB130 by deleting the static protection diodes on DDC_SCL (D4) and DDC_SDA (D1) and replacing them with 15-kΩ resistors.

Current DECchip 21130 Pin List

If you have a *DECchip 21130 PCI Integrated Graphics and Video Accelerator Technical Reference Manual* dated before May 10, 1995, use the following pin list until you receive an updated reference manual:

Pin Number	Single Name	Function
1	MEMDATA<13>	B
2	MEMDATA<12>	B
3	MEMDATA<11>	B
4	MEMDATA<10>	B
5	VSS(Video)	Power
6	VDD(Video)	Power
7	MEMDATA<09>	B
8	MEMDATA<08>	B
9	MEMDATA<07>	B
10	MEMDATA<06>	B
11	MEMDATA<05>	B
12	MEMDATA<04>	B
13	MEMDATA<03>	B
14	MEMDATA<02>	B
15	MEMDATA<01>	B
16	MEMDATA<00>	B
17	VSS(AC)0	Power
18	VAFC_EN#	O
19	EVIDEO#	I
20	VSYNC	B
21	HSYNC	B
22	BLANK#	B
23	VAFC_VCLK	I
24	GRDY	B
25	VAFC_DCLK	B
26	VDD(Core)0	Power
27	VSS(Core)0	Power
28	PIXCLK	I
29	PLL_TEST	B

Pin Number	Signal Name	Function
30	DDC_IN	I
31	TEST_IN	I
32	PLL_VSS	Power
33	FILTER	Bt/I
34	PLL_VDD	Power
35	PLL_VSS	Power
36	XTAL2	Bt/I
37	XTAL1	Bt/I
38	PLL_VSS	Power
39	FSADJUST	Bt/I
40	VREFIN	Bt/I
41	OPA_VDD	Power
42	DAC_VDD	Power
43	COMP	Bt/I
44	OPA_VSS	Power
45	IOB	Bt/O
46	DAC_VSS	Power
47	IOG	Bt/O
48	DAC_VSS	Power
49	IOR	Bt/O
50	DAC_VSS	Power
51	VSS(PCI) 0	Power
52	VDD(PCI) 0	Power
53	PCI_INTA#	PCI/OD
54	PCI_RST#	PCI/I
55	PCI_GNT#	PCI/I
56	PCI_REQ#	PCI/B
57	PCI_AD<31>	PCI/B
58	PCI_AD<30>	PCI/B
59	PCI_AD<29>	PCI/B
60	PCI_AD<28>	PCI/B
61	VSS(PCI) 1	Power
62	VDD(PCI) 1	Power
63	PCI_AD<27>	PCI/B
64	PCI_AD<26>	PCI/B
65	PCI_AD<25>	PCI/B
66	PCI_AD<24>	PCI/B
67	PCI_CBE<3>#	PCI/B
68	PCI_IDSEL	PCI/I
69	PCI_AD<23>	PCI/B
70	VDD(PCI) 2	Power
71	VSS(PCI) 2	Power
72	PCI_AD<22>	PCI/B
73	PCI_AD<21>	PCI/B
74	PCI_AD<20>	PCI/B

Pin Number	Signal Name	Function
75	PCI_AD<19>	PCI/B
76	PCI_AD<18>	PCI/B
77	PCI_AD<17>	PCI/B
78	PCI_AD<16>	PCI/B
79	VDD(PCI) 3	Power
80	VSS(PCI) 3	Power
81	PCI_CLK	PCI/I
82	VSS(PCI) 4	Power
83	PCI_CBE<2>#	PCI/B
84	PCI_FRAME#	PCI/B
85	PCI_IRDY#	PCI/B
86	PCI_TRDY#	PCI/B
87	PCI_DEVSEL#	PCI/B
88	PCI_STOP#	PCI/B
89	PCI_PERR	PCI/B
90	PCI_SERR	PCI/OD
91	PCI_PAR	PCI/B
92	VDD(PCI) 4	Power
93	VSS(PCI) 5	Power
94	PCI_CBE<1>#	PCI/B
95	PCI_AD<15>	PCI/B
96	PCI_AD<14>	PCI/B
97	PCI_AD<13>	PCI/B
98	PCI_AD<12>	PCI/B
99	PCI_AD<11>	PCI/B
100	PCI_AD<10>	PCI/B
101	PCI_AD<09>	PCI/B
102	PCI_AD<08>	PCI/B
103	VDD(PCI) 5	Power
104	VSS(PCI) 6	Power
105	PCI_CBE<0>#	PCI/B
106	PCI_AD<07>	PCI/B
107	PCI_AD<06>	PCI/B
108	PCI_AD<05>	PCI/B
109	PCI_AD<04>	PCI/B
110	PCI_AD<03>	PCI/B
111	PCI_AD<02>	PCI/B
112	PCI_AD<01>	PCI/B
113	PCI_AD<00>	PCI/B
114	VDD(PCI) 6	Power
115	VSS(PCI) 7	Power
116	GP_CS#	O
117	GP_RESET#	O
118	GP_INT	I
119	GP_STB#	O

Pin Number	Signal Name	Function
120	ROM_CE#	O
121	VGAFC_DATA<0>	B
122	VGAFC_DATA<1>	B
123	VGAFC_DATA<2>	B
124	VDD(AC)0	Power
125	MEMDATA<63>	B
126	MEMDATA<62>	B
127	MEMDATA<61>	B
128	MEMDATA<60>	B
129	MEMDATA<59>	B
130	MEMDATA<58>	B
131	MEMDATA<57>	B
132	MEMDATA<56>	B
133	VSS(AC) 1	Power
134	MEMDATA<55>	B
135	MEMDATA<54>	B
136	MEMDATA<53>	B
137	MEMDATA<52>	B
138	MEMDATA<51>	B
139	MEMDATA<50>	B
140	MEMDATA<49>	B
141	MEMDATA<48>	B
142	VSS(DC)0	Power
143	VDD(DC)0	Power
144	MEMDATA<47>	B
145	MEMDATA<46>	B
146	MEMDATA<45>	B
147	MEMDATA<44>	B
148	MEMDATA<43>	B
149	MEMDATA<42>	B
150	MEMDATA<41>	B
151	MEMDATA<40>	B
152	MEMDATA<39>	B
153	VDD(AC)1	Power
154	MEMDATA<38>	B
155	MEMDATA<37>	B
156	MEMDATA<36>	B
157	MEMDATA<35>	B
158	MEMDATA<34>	B
159	MEMDATA<33>	B
160	MEMDATA<32>	B
161	VDD(DC)1	Power
162	VSS(DC)1	Power
163	MEMADDR<8>	O

Pin Number	Signal Name	Function
164	MEMADDR<7>	O
165	MEMADDR<6>	O
166	MEMADDR<5>	O
167	MEMADDR<4>	O
168	MEMADDR<3>	O
169	MEMADDR<2>	O
170	MEMADDR<1>	O
171	MEMADDR<0>	O
172	VSS(AC)2	Power
173	OEB#	O
174	CAS<7>#	O
175	CAS<6>#	O
176	CAS<5>#	O
177	CAS<4>#	O
178	CAS<3>#	O
179	VDD(Core)1	Power
180	VSS(Core)1	Power
181	CAS<2>#	O
182	CAS<1>#	O
183	CAS<0>#	O
184	RAS<2>#	O
185	RAS<1>#	O
186	RAS<0>	O
187	VSS(AC)3	Power
188	WRB#	O
189	MEMDATA<31>	B
190	MEMDATA<30>	B
191	MEMDATA<29>	B
192	MEMDATA<28>	B
193	MEMDATA<27>	B
194	MEMDATA<26>	B
195	VDD(AC)2	Power
196	MEMDATA<25>	B
197	MEMDATA<24>	B
198	MEMDATA<23>	B
199	MEMDATA<22>	B
200	MEMDATA<21>	B
201	MEMDATA<20>	B
202	MEMDATA<19>	B
203	VSS(AC)4	Power
204	MEMDATA<18>	B
205	MEMDATA<17>	B
206	MEMDATA<16>	B
207	MEMDATA<15>	B
208	MEMDATA<14>	B

Technical Support and Ordering Information

Technical Support

If you need technical support or help deciding which literature best meets your needs, call the Digital Semiconductor Information Line:

United States and Canada	**1-800-332-2717**
TTY (United States only)	**1-800-332-2515**
Outside North America	**+1-508-568-6868**

Ordering Associated Digital Semiconductor Literature

The following table lists some of the available Digital Semiconductor literature. For a complete list, contact the Digital Semiconductor Information Line.

Title	Order Number
DECchip 21130 PCI Integrated Graphics and Video Accelerator Technical Reference Manual	EC−QD2QB−TE
DECchip 21130 PCI Integrated Graphics and Video Accelerator Compatible Memory Devices: An Application Note	EC−QLEGB−TE

Ordering Third-Party Literature

You can order the following third-party literature directly from the vendor:

Title	Vendor
PCI Local Bus Specification Revision 2.0	PCI Special Interest Group 5200 NE Elam Young Pkwy Hillsboro, OR 97124-6497 1-503-696-2000
VESA Standard VGA Pass-Through Connector VS890803	VESA 2150 N First Street, Suite 440 San Jose, CA 95131-2029 FAX 1-408-435-8225
VESA Display Power Management Signaling (DPMS)	See previous entry.
VESA Display Data Channel (DDC™) Standard	See previous entry.