Digital Semiconductor

Alpha 21068 Microprocessor

Product Brief

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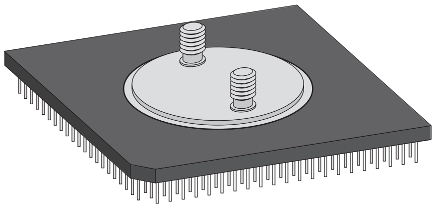

Description

The Alpha 21068 microprocessor is a highly-integrated implementation of Digital's Alpha architecture for high-performance, embedded applications. Onchip functions include industry-standard PCI I/O controller, fully pipelined integer and floating-point processors, memory controller, graphics accelerator, instruction and data caches, and external cache controller.

Features

- 64-bit, fully pipelined, advanced RISC architecture supported by multiple operating systems
- An evaluation board (EB66) is available and supports:
  - Microsoft Windows NT
  - OSF/1
- Best-in-class performance
  - 66-MHz operation
  - Superscalar (dual issue)
  - Peak instruction execution rate of 133 million instructions per second
  - 0.68-µm CMOS technology
- Pipelined floating-point unit
  - IEEE single- and double-precision, VAX F_floating and G_floating, longword and quadword data types
- Memory management
  - Demand-paged
  - 12-entry instruction-stream translation buffer (TB), eight entries map 8KB pages, four entries map 8KB to 4MB pages
  - 32-entry data-stream TB, each entry maps 8KB, 64KB, 512KB, or 4MB pages
- High-bandwidth memory controller
  - Full 64-bit memory data path
  - DRAM controller for four banks of memory with fully programmable timing and error correction code (ECC)
  - RAS/CAS memory bus to industry-standard SIMMs
- External secondary write-back cache controller
  - Direct connection to SRAM with no external logic required
  - Programmable cache size and speed
- Onchip, 8KB, direct-mapped, write-through data cache
- Onchip, 8KB, direct-mapped instruction cache
- Embedded graphics accelerator
  - High-bandwidth memory data path to video RAM (VRAM)
  - Onchip support for direct connection to VRAM frame buffer
- PCI I/O controller
  - No external logic needed to connect PCI-compliant components
  - High DMA bandwidth
  - 32-bit multiplexed address/data
  - DMA reads and writes
  - Scatter-gather map support for DMA
  - Asynchronous operation to CPU
  - Multimaster with peer-to-peer access
- Privileged architecture library code (PALcode) supports:
  - Optimization for multiple operating systems
  - Flexible memory-management implementations
  - Multi-instruction atomic sequences
- Advanced packaging technology for superior thermal management performance
- Built-in phase-locked loop (PLL)
  - Frequency multiplier that allows low-cost input clock
  - Programmable multiplier values
- Serial ROM (SROM) interface
  - Loads instruction cache after reset
  - Allows software-controlled serial port after initialization
- Chip- and module-level test support for JTAG (IEEE 1149)
- 3.3-V I/O supply voltage with chip interface directly to 5-V logic
- Pin compatible with 21066 and 21066A
- Software compatible with 21064A, 21066, 21066A, and 21164

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ALPHA GENERATION™

Alpha 21068 Microprocessor Microarchitecture

The Alpha 21068 microprocessor uses a 7-stage pipeline for integer operate and memory reference instructions, and a 10-stage pipeline for floating-point operate instructions. The instruction fetch and decode unit (IFDU) maintains state for all pipeline stages to track outstanding register writes.

Figure 1 shows the CPU and the integrated system support features of the 21068.

The CPU

The CPU contains:

Instruction Cache (Icache) — The Icache is an 8KB direct-mapped, physically-addressed cache with 32-byte blocks.

Instruction Fetch and Decode Unit (IFDU) — The IFDU includes the instruction translation buffers (ITBs) and the branch prediction logic (branch unit). The IFDU performs instruction fetch, resource checks, and dual instruction issue to the IEU, LSU, FPU, or branch unit. The IFDU also controls pipeline bypasses, stalls, aborts, and restarts.

Integer Execution Unit (IEU) — The IEU contains a 64-bit, fully pipelined integer execution data path, including adder, logic box, barrel shifter, byte extract and mask, and independent integer multiplier. The IEU also contains the 32-entry, 64-bit integer register file (IRF).

Floating-Point Unit (FPU) — The FPU contains a fully pipelined floating-point unit and independent divider. IEEE single-precision and double-precision floating-point data types are supported. VAX F_floating and G_ floating data types are fully supported, and there is limited support for the VAX D_floating data type. The FPU also contains a 32-entry, 64-bit floating-point register file (FRF).

Load and Store Unit (LSU) —The LSU contains four major sections: address translation data path, which includes the data translation buffer (DTB); load silo; write buffer; and Dcache interface. The LSU supports all integer and floating-point load and store instructions, including address calculation and translation, and cache control logic.

Data Cache (Dcache) — The Dcache is an 8KB, write-through, read-allocate, direct-mapped, physically-addressed cache with 32-byte blocks.

The Integrated System

The integrated system support features of the 21068 include:

PCI I/O Controller (IOC) — The IOC functions as an interface bridge between peripheral devices and the CPU and system memory. The IOC interface protocol is compliant with the peripheral component interconnect (PCI) specification. Peripheral chips that interface to PCI can be connected to the 21068 without any external logic.

Scatter-gather mapping logic translates the 32-bit addresses generated by PCI bus masters to the 34-bit CPU address space. An 8-entry translation look-aside buffer (TLB) provides fast translations. The scatter-gather map tables, stored in system memory for low cost, are automatically read by the IOC when a translation misses in the TLB.

Memory Controller — The memory controller supports one to four banks of DRAM/VRAM and/or SRAM. Timing is fully programmable, as are RAM size, ECC, write-per-bit, and split bank. Up to 512MB of physical memory can be configured. The memory controller also includes the graphics accelerator and external cache support. External cache can be programmed for speed, size, and ECC.

External Cache — The 21068 supports an optional external cache built from off-the-shelf SRAMs. The external cache is a write-back, read-allocate cache with 8-byte blocks. The chip directly controls the SRAMs using its programmable external cache interface. This allows each implementation to select its own external cache speed and configuration. The programmable interface supports cache sizes from 64KB to 2MB and a range of operating speeds that are submultiples of the chip clock.

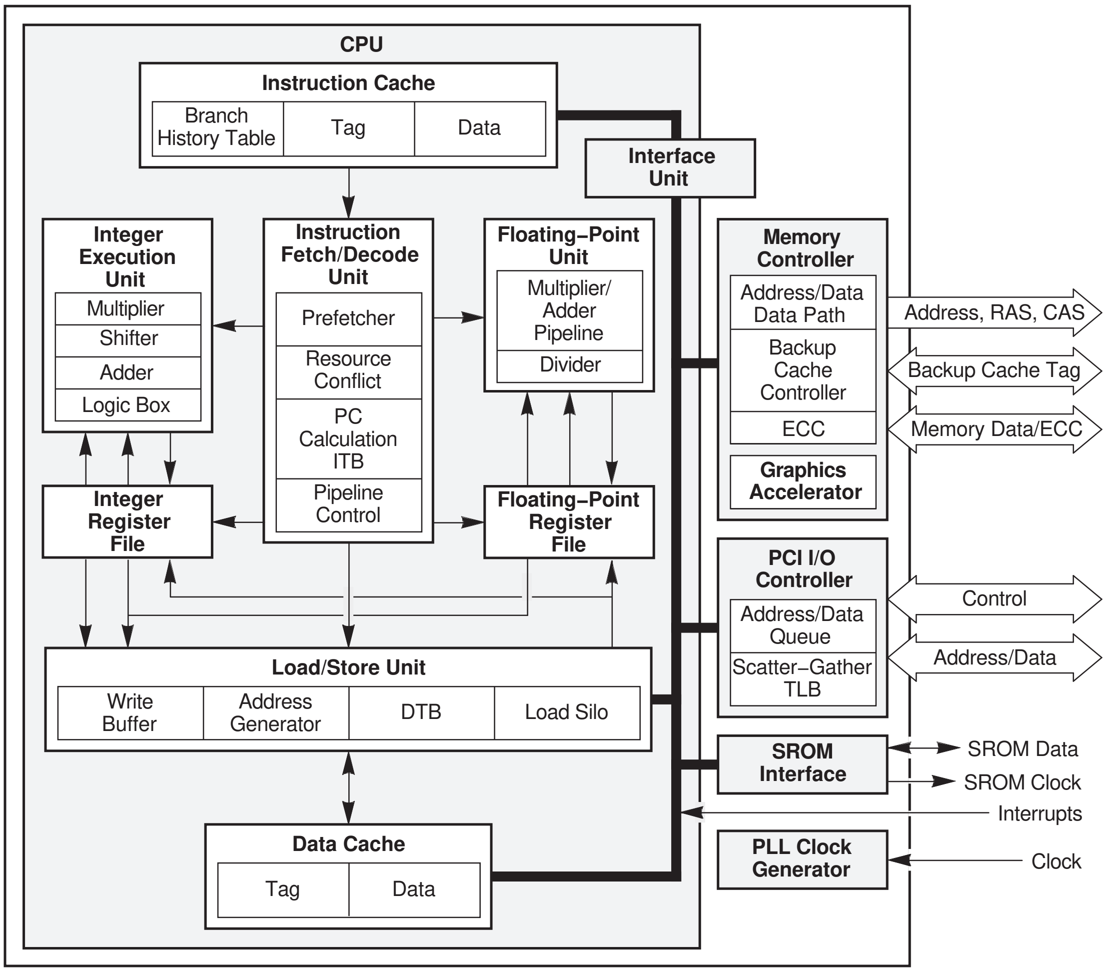
Virtual Address Space — The virtual address is a 64-bit unsigned integer that specifies a byte location in the virtual address space. The microprocessor implements a 43-bit subset of the virtual address space and supports a 34-bit, 16GB physical address space.

Graphics Accelerator — The graphics accelerator operates on 1-, 2-, 4-, 8-, 16-, or 32-plane frame buffers. It includes pixel control, transparent stipple, and foreground data. With external video timing, the memory controller does VRAM data transfer cycles using an onchip address counter.

Serial ROM (SROM) Interface — This interface loads the instruction cache after reset. It has a software-controlled serial port, which is activated after initialization. The SROM supports system-level design debug.

PLL Clock Generator — The built-in phase-locked loop (PLL) has a frequency multiplier that allows usage of a low-cost input clock.

Figure 1 Alpha 21068 Microprocessor Block Diagram



Alpha Architecture Summary

As implemented in the 21068, the Alpha architecture supports:

- A fixed 32-bit instruction size
- Separate integer and floating-point registers
  - Thirty-two 64-bit integer registers
  - Thirty-two 64-bit floating-point registers
- 32-bit (longword) and 64-bit (quadword) integer data types
- 32-bit and 64-bit IEEE and VAX floating-point data types
- Memory accesses using a 64-bit virtual byte address
- Privileged architecture library code (PALcode)

Instruction Set

All instructions are 32 bits long and use one of four different instruction formats (see Figure 2). Each format uses a 6-bit opcode and zero, one, two, or three 5-bit register fields.

CALL_PAL Instruction
CALL_PAL instructions vector to a privileged layer of software that atomically performs both privileged and unprivileged functions.

Branch Instructions
Conditional branch instructions test a register for positive/negative, zero/nonzero, or even/odd conditions, and perform a PC-relative branch. Unconditional branch instructions perform either an absolute or PC-relative jump using an arbitrary 64-bit register value. They can update a destination register with a return value.

Load and Store Instructions
Load and store instructions can move either 32-bit or 64-bit quantities. The 8-bit and 16-bit load/store operations are supported through an extensive set of in-register byte manipulations. The I/O bus directly supports byte and word operations in hardware.

Operate Instructions
Integer operate instructions manipulate full 64-bit values and include a full complement of arithmetic, compare, logical, and shift instructions. There are also three 32-bit integer operates: add, subtract, and multiply.

In addition to conventional RISC operations, the instruction set provides scaled add and subtract for quick subscript calculation; 128-bit multiply for multiprecision arithmetic and division by a constant; conditional moves for avoiding branches; and an extensive set of in-register byte manipulation instructions.

Floating-point operate instructions include four complete sets of instructions for IEEE single-precision, IEEE double-precision, VAX F_floating, and VAX G_floating arithmetic. In addition to arithmetic instructions, there are instructions for conversions between floating and integer values, including the VAX D_floating data type.

PALcode

PALcode is a privileged layer of software that automatically performs such functions as the dispatching and servicing of interrupts, exceptions, task switching, and additional privileged and unprivileged user instructions as specified by operating systems using the CALL_PAL instruction.

PALcode is the only method of performing some operations on the hardware. In addition to the instructions defined by the Alpha architecture, a set of implementation-specific instructions is provided.

PALcode runs in an environment with privileges enabled, instruction stream mapping disabled, and interrupts disabled. Disabling memory mapping allows PALcode to support functions such as translation buffer miss routines. Disabling interrupts allows the instruction stream to provide multi-instruction sequences as atomic operations.

Memory Management

The memory-management architecture provides:

- A large address space for instructions and data
- Convenient and efficient sharing of instructions and data
- Independent read and write access protection
- Flexibility through programmable PALcode support

Figure 2 Alpha Instruction Formats

	31–26	25–21	20–16	15–5	4–0
CALL_PAL	Opcode	Function			
Branch	Opcode	Ra	Displacement		
Load/Store	Opcode	Ra	Rb	Displacement	
Operate	Opcode	Ra	Rb	Function	Rc

Adding the 21068 to Your Design Strategy

The 21068 reduces the overall cost of system development, provides for easier system design, and provides the benefits of high performance by bringing the Alpha architecture to embedded systems.

By using the 21068, your designs can benefit in the following ways:

Easy Migration of Custom PCI Peripherals

Because the 21068 is designed with a high DMA bandwidth PCI I/O controller that interfaces to industry-standard PCI components, you'll have investment protection for the custom PCI peripherals you're designing with today — through successive generations of Alpha microprocessors.

Flexibility of Memory Design

The 21068 is highly integrated to free up board real estate and reduce the cost of designing. You can make market-driven system design decisions using the integrated memory controller that interfaces with up to 512MB of industry-standard DRAM or VRAM. Memory can be configured into as many as four banks with fully programmable bank size, timing, and error correction code (ECC).

Optimizing System Performance

The secondary cache controller on the 21068 is used for optional, external secondary cache that uses industry-standard SRAMs. The flexibility of the secondary cache size and speed allows you to optimize your system performance.

Plug-and-Go Graphics

The 21068 provides onchip support for direct connection to a VRAM frame buffer, providing graphics capability at low cost.

Flexibility of Design

The 21068 interfaces directly to components operating at a supply voltage of 3.3 V or 5 V. This means you can use the standard 5-V components that best fit your applications and market demands.

The 21068 has a built-in phase-locked loop (PLL) clock multiplier that allows system designs at a comfortable frequency of 25 or 33 MHz, so designers can continue to use existing design strategies and familiar components.

ISO 9002 Certification

All of Digital's semiconductor manufacturing sites adhere to the stringent ISO 9002 standards and are ISO 9002 certified.

Longevity of Design

All Alpha microprocessors are designed to the Alpha architecture. So whether your design requires the high speed and performance of the 21064, or the power and cost sensitivity of the 21068 and 21066, your designs will be assured of compatibility across this family of high-performance Alpha microprocessors.

Technology Leadership

Designing with Digital's Alpha microprocessors puts you in a place of leadership in the industry. Your products will benefit from the unbounded capacity of 64-bit technology, the built-in longevity of the Alpha architecture, and Digital's commitment to constant improvement in price/performance through the company's investment in semiconductor design and fabrication.

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Characteristics	
Characteristic	**Specification**
Power supply	Vss 0.0 V Vdd 3.3 V ±5% Vcc (pll_5V) 5.0 V ±5%
Operating temperature	Tj maximum = 100°C
Storage temperature range	–55°C to 125°C
Power dissipation @ Vdd = 3.46 V and Frequency = 66 MHz	9 W maximum
Package	287-pin PGA with 0.10-in grid spacing and advanced thermal technology

For More Information

To learn more about the availability of the Alpha 21068 microprocessor, contact your local semiconductor distributor. To learn more about Digital Semiconductor's product portfolio, contact the Digital Semiconductor Information Line:

1-800-332-2717
1-800-332-2515 (TTY)

Outside North America, call:

+1-508-568-6868

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