DECchip 21064 and DECchip 21064A PCI Evaluation Board Design Package

Read Me First

Order Number: EC–QCJGA–TE

Revision/Update Information: This is a revised document.

Digital Equipment Corporation
Maynard, Massachusetts

September 1994

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1 Introduction to the DECchip 21064 PCI Evaluation Board Kit

The DECchip 21064 PCI Evaluation Board Kit is an evaluation and development module designed to introduce you to the DECchip 21064 or the DECchip 21064A Alpha AXP microprocessor and to help you learn more about designing the chip into your products. This evaluation board also provides a platform for peripheral component interconnect (PCI) I/O device hardware and software development. Using the DECchip 21064 PCI Evaluation Board (also called the EB64+), you will be able to do the following:

- Validate the DECchip 21064 or DECchip 21064A for ease of use and setup.
- Evaluate the DECchip 21064 or DECchip 21064A for speed and cost per performance.
- Evaluate the DECchip 21071 and DECchip 21072 chipsets.
- Provide a PCI interface to the DECchip 21064 or DECchip 21064A.
- Develop software tools by using and modifying the tools provided in the kit.
- Create new designs by using the examples in the kit.
- Use the documentation to learn more about the DECchip 21064 and DECchip 21064A microprocessors, the EB64+, and Alpha AXP architecture.

The EB64+ also supports a variety of CPU speeds. While the evaluation board is purchased with a 200 MHz or 275 MHz microprocessor, it supports speeds of 150 MHz and up. The following sample kits are available for purchase:

Table 1 Sample Kits

Product	Speed	Order Number
DECchip 21064–150 Sample Kit	150 MHz	21064–SA
DECchip 21064–166 Sample Kit	166 MHz	21064–SC
DECchip 21064–200 Sample Kit	200 MHz	21064–SB
DECchip 21064A–233 Sample Kit	233 MHz	21064–SD
DECchip 21064A–275 Sample Kit	275 MHz	21064–SE

Each sample kit contains a microprocessor, heat sink assembly, oscillators, and a blank SROM. Please contact your Digital sales representative or call 1–800–DIGITAL for ordering information.

This document, *DECchip 21064 and DECchip 21064A PCI Evaluation Board Design Package Read Me First*, provides an overview of the kit contents and gives some information about how to begin using the EB64+.

2 Kit Contents

The DECchip 21064 PCI Evaluation Board Kit contains the following:

- The DECchip 21064 PCI Evaluation Board (EB64+) with a debug ROM
- The Alpha AXP Evaluation Board Software Developers Kit (provided on 3½-inch diskettes and a 4 mm - 60 m DAT cassette)
  - Software tools for use with a Windows NT or OSF/1 host system
  - Firmware sources
  - PALcode sources
  - Documentation (hardcopy)
- The DECchip 21064 and DECchip 21064A PCI Evaluation Board Design Package (provided on 3½-inch diskettes and a 4 mm - 60 m DAT cassette)
- DECchip 21064 and DECchip 21064A PCI Evaluation Board Documentation Set
- DECchip 21064/21066/21068 PCI Evaluation Board Accessories Kit

2.1 System Requirements

The EB64+ derives its main system power from a user-supplied, industry-standard PC power supply. The power supply you select for your EB64+ depends on how you plan to configure your system. For a system that includes a controller, a disk, a speaker, and an external interface, a 230-watt power supply should suffice. For more information, see the Board Requirements and Parameters chapter in the *DECchip 21064 and DECchip 21064A Alpha AXP PCI Evaluation Board User's Guide*.

3 Documentation Provided

The following documentation is included in the DECchip 21064 PCI Evaluation Board Kit.

Title	Order Number
DECchip 21064 Literature	
Alpha Architecture Handbook	EC–H1689–10
DECchip 21064–150, –166, –200 Alpha AXP Microprocessor Data Sheet	EB–N0136–72
DECchip 21064A Alpha AXP Microprocessor Data Sheet	EC–N0699–72
DECchip 21064A Alpha AXP Microprocessor Product Brief	EC–N0698–72
DECchip 21064 and DECchip 21064A Alpha AXP Microprocessors Hardware Reference Manual	EC–Q9ZUA–TE
SPICE models for Alpha AXP Microprocessor and Peripheral Chips: An Application Note	QR–21B02–30
Designing a System with the DECchip 21064 Microprocessor: An Application Note	EC–N0107–72
Alpha AXP Evaluation Board Software Documentation	
PALcode for Alpha AXP Microprocessors System Design Guide	EC–N0660–72
Alpha AXP Evaluation Board Debug Monitor User’s Guide	EC–N0661–72
Alpha AXP Evaluation Board Software Design Tools User’s Guide	EC–N0662–72
Alpha AXP SROM Mini-Debugger User’s Guide	EC–N0750–72
DECchip 21064 PCI Evaluation Board Literature	
DECchip 21064 and DECchip 21064A PCI Evaluation Board Design Package Read Me First	EC–QCJGA–TE
DECchip 21064 and DECchip 21064A Alpha AXP PCI Evaluation Board Product Brief	EC–N0639–72
DECchip 21064 and DECchip 21064A Alpha AXP PCI Evaluation Board User’s Guide	EC–N0640–72

Title	Order Number
Associated DECchip Documentation	
DECchip 21040 Ethernet LAN Controller for PCI Product Brief	EC–N0281–72
DECchip 21040 Ethernet LAN Controller for PCI Data Sheet	EC–N0280–72
DECchip 21071 and DECchip 21072 Core Logic Chipsets Product Brief	EC–N0637–72
DECchip 21071 and DECchip 21072 Core Logic Chipsets Data Sheet	EC–QAEMA–TE

4 Choosing a Design Strategy

How you use the DECchip 21064 PCI Evaluation Board depends on how you plan to design a system or evaluate the DECchip 21064 or DECchip 21064A. The following table provides some guidelines to help you determine which documentation and software you need to accomplish what you want.

If you want to...	Start with these...
Use the EB64+ without making changes.	• DECchip 21064 and DECchip 21064A Alpha AXP PCI Evaluation Board User's Guide • Alpha AXP Evaluation Board Debug Monitor User's Guide
Use the EB64+ and modify either the firmware or the software.	• DECchip 21064 and DECchip 21064A Alpha AXP PCI Evaluation Board User's Guide • Alpha AXP Evaluation Board Debug Monitor User's Guide • Source files • Software tools • Alpha AXP Evaluation Board Software Design Tools User's Guide
Design new hardware with the DECchip 21064.	• DECchip 21064 and DECchip 21064A Alpha AXP PCI Evaluation Board User's Guide • Alpha AXP Evaluation Board Debug Monitor User's Guide • Source files • Software tools • Alpha AXP Evaluation Board Software Design Tools User's Guide • Hardware design database • Alpha AXP SROM Mini-Debugger User's Guide

5 Connecting the DECchip 21064 PCI Evaluation Board

The DECchip 21064 PCI Evaluation Board can be connected to a terminal or Alpha AXP hardware running the Windows NT or OSF/1 operating system. The EB64+ is configured to operate without any changes by the user. To connect your EB64+ to a power source and a terminal, follow this procedure:

1. Refer to Chapter 2 in the *DECchip 21064 PCI Evaluation Board User's Guide* to learn about the board's connectors and jumpers.
2. Connect your terminal to serial communications port 1, connector J12.
3. Connect your standard PC power supply to connectors J2 and J3.
4. Refer to Chapter 2 in the *Alpha AXP Evaluation Board Debug Monitor User's Guide* for information about setting up serial port and Ethernet communication.

5.1 Choosing the Media

The DECchip 21064 PCI Evaluation Board Design Package database, the software tools, and the PALcode are provided in machine-readable form. The following table will help you determine which medium to copy your files from.

If your development system is...	Then use this medium...	To do...
A DEC 3000 Model 500 AXP workstation running the OSF/1 operating system	The DAT cassettes to copy the hardware design database, the software tools, and the PALcode on to your system	Hardware and software design and development
A DEC 2000 Model 300 AXP running the Windows NT operating system	The Windows NT Software Tool diskettes to copy the Windows NT software tools onto your system	Software design and development
A DOS-based PC with a 3½-inch diskette drive	The EB64+ Design Database diskettes to copy the hardware design database onto your system	Hardware design development

6 The Hardware Design Package Database

The DECchip 21064 PCI Evaluation Board Design Package contains the following information and files:

- Complete hardware design database (on 3½-inch diskettes and DAT cassette)
  - Vendors parts list
  - Schematics in PostScript files and in a Viewsim database
  - Gerber files
  - ABEL source files (including PLD equations)

6.1 Copying and Unpacking the Hardware Design Database from the DAT Cassette

The hardware design database provided on DAT cassette is in a tar file called `eb64p_db.tar`.

To copy and unpack the tar file, follow this procedure:

1. Enter this command to copy `eb64p_db.tar` from the DAT cassette to the current directory on your system:

   ```
   tar xv eb64p_db.tar
   ```

2. Enter this command to unpack the tar file:

   ```
   tar xvf eb64p_db.tar
   ```

   This command creates an `archive` area and unpacks all the files in the correct places for Viewlogic operation, including design and simulation.

3. Set the `archive` area as the current default work area.
4. Include the following Viewlogic library areas in the search path:
   - builtin
   - dio (this is available with the ViewPLD option)

6.2 Copying and Unpacking the Hardware Design Database from the Diskettes

The four 3½-inch diskettes that contain the hardware design database files were archived using PKZIP. Each zip archive includes a category of design database files, which are described in the table in the following section. You can access and read these files on an industry-standard personal computer with a 3½-inch diskette drive. Use PKUNZIP to unpack the files in each archive.

6.3 Files on the Diskettes

The hardware design database diskettes contain the following files:

Archive Name	Archive Contents	Comments
Disk 1		
t1_read.me	Provides a general description of the diskette contents.	This file does not need to be unpacked.
eb64pps1.zip	Contains all the layer plots, soldermask plots, silkscreen plots and solderpaste plots necessary to manufacture the EB64+.	These files are B-size (11 in x 17 in) PostScript files.
Disk 2		
t2_read.me	Provides a general description of the diskette contents.	This file does not need to be unpacked.
eb64pps2.zip	Contains the unit assembly drawings for the EB64+.	The assembly drawings provide a pictorial representation of the EB64+, with component designations for each device.
eb64pbrd.zip	Contains all the necessary files to have the EB64+ printed circuit board fabricated.	–
eb64pbom.zip	Contains the EB64+ parts list.	This file references Digital part numbers.
venbom.zip	Contains the EB64+ parts list.	This file references vendor part numbers.
eb64pwir.zip	Contains all the wirelist files.	Copy this file to the /WIR Viewlogic database subdirectory.

Archive Name	Archive Contents	Comments
Disk 3		
t3_read.me	Provides a general description of the diskette contents.	This file does not need to be unpacked.
eb64pps.zip	Contains the PostScript file of the EB64+ board-level schematics.	These files are not needed to simulate and are provided for information. You can create the same files using the database provided.
Disk 4		
t4_read.me	Provides a general description of the diskette contents. These files were generated with Powerview Version 5.1.1.	This file does not need to be unpacked.
eb64ppal.zip	Contains the industry-standard JEDEC files that were used to program all the PAL components and MACH devices.	These files are not needed to simulate and are included only to provide you with the ability to recreate all of the programmable devices on the module.
eb64psch.zip	Contains schematic files for the EB64+ Viewlogic schematic database.	Copy this file to the /SCH Viewlogic database subdirectory.
eb64psym.zip	Contains symbol files for the EB64+ Viewlogic schematic database.	Copy this file to the /SYM Viewlogic database subdirectory.
eb64pxrf.zip	Contains the cross reference file for the EB64+ Viewlogic schematic database.	–

7 The Alpha AXP Evaluation Board Software Developers Kit

The Alpha AXP Evaluation Board Software Developers Kit is supplied on DAT cassette and is also supplied on five 3½-inch diskettes.

7.1 Copying and Unpacking the Software Developers Kit from the DAT Cassette

The software developers kit is provided in a tar file. The approximate expanded size of the DAT cassette is 85 megabytes. To unpack and copy this file from the DAT cassette to the current directory on your system, enter this command:

```
tar xv
```

This command creates the following files and subdirectories.

Directory Name	Directory Contents	Comments
README	Provides a general description of all the directories contained on the DAT tape.	–
ebfw	Contains the source files to rebuild firmware.	This includes the debug monitor and PALcode. See the included readme file for more information.
ebroms	Contains the Motorola S-record and Intel MCS-86 hex files used to program the ROMs contained in the evaluation board.	Also contains the mini_dbg.hex file (SROM Mini-Debugger) ready to be programmed into an 1736A serial ROM or equivalent.
tools	Contains the executable images of the evaluation board toolset for use on OSF/1 and Windows NT operating system.	See the included readme file for more information.
infozip	Contains the compression utility used to make the zip files on the diskettes (sources and executables).	This utility is compatible with PKZIP.

7.2 Copying and Unpacking the Software Developers Kit from the Diskettes

The software developers kit was archived and the compression utility is included on the diskettes. These diskettes are intended for use with the Windows NT operating system.

The software design kit diskettes contain the following files.

Archive Name	Archive Contents	Comments
Disk 1		
README	Provides a general description of the contents of all the diskettes.	This file does not need to be unpacked.
nt_tools.zip	Contains the executable images of the evaluation board toolset for use on the Windows NT operating system.	–
unzip.exe	Contains compression utility unzip file.	This file is used to unzip the zip files contained on these diskettes.
Disk 2		
ebfw.zip	Contains the source files to rebuild firmware.	This includes the debug monitor and PALcode.
Disk 3		
infozip.zip	Contains the compression utility sources.	–
utils.zip	Contains the source files used to rebuild most of the evaluation board toolset.	A readme file is also included to describe the tools, the location of the sources, and instructions for building.
Disk 4		
nt_gnu.zip	Contains the source files used to rebuild the GNU tools.	Supplied to comply with the Free Software Foundation license. You should not need to modify these sources. These files are buildable on the Windows NT operating system.

Archive Name	Archive Contents	Comments
Disk 5		
roms.zip	Contains the Motorola S-record and Intel MCS-86 hex files used to program the ROMs contained in the evaluation board. This diskette also contains the hex file for the SROM mini-debugger.	The Motorola S-records file is ready to be programmed into a 27C040 EPROM or equivalent. The Intel MCS-86 hex file is ready to be programmed into an 1736A serial ROM or equivalent.

8 Alpha AXP Debug Monitor and Debug Monitor Source Files

The EB64+ comes with a debug ROM. This ROM, automatically read into memory after reset, provides a command line interface that can be used to

- Download files via serial and Ethernet ports, ROM socket, and user supplied floppy drive.
- Read and write memory and I/O.
- Examine and deposit the CPU IPRs and I/O mapped registers.
- Examine and modify DRAM and I/O mapped memory.
- Transfer control to programs loaded into memory.
- Perform native debugging, including breakpoints and single stepping.
- Perform full source-level debugging using DECladebug running on a remote host that communicates through an Ethernet connection.

The *Alpha AXP Evaluation Board Debug Monitor User's Guide* describes how to use the onboard debug ROM.

9 Software Tools

The software tools provided for EB64+ software development require an Alpha AXP system running the Windows NT or OSF/1 operating system. Both the Windows NT and OSF/1 operating systems provide tools that can be used in conjunction with the evaluation board tools provided in this kit. These tools allow you to build, modify, and or develop software for your evaluation board.

9.1 Alpha AXP Evaluation Board Software Tools Kit Contents

The following table lists the tools that have been created or modified for the Alpha AXP Evaluation Board Software Tools Kit.

Tool Name	Description	Operating System
GAS	GNU-based assembler	OSF/1, Windows NT
ALIST	Generates a listing file from C source and its associated assembler	OSF/1, Windows NT
ASTRIP	Strips header information from an a.out format executable file	OSF/1, Windows NT
CLIST	Produces a listing from coff format	OSF/1
CSTRIP	Strips header information from a coff format executable file	OSF/1
PVC	Checks for PALcode Violation	OSF/1, Windows NT
SROM	Embeds instruction cache initialization into the executable data and generates Intel Hex format	OSF/1, Windows NT
SREC	Takes an arbitrary image and converts it to Motorola S-record format	OSF/1, Windows NT
SYSGEN	Concatenates the specified input files into one contiguous image	OSF/1, Windows NT
MAKEROM	Builds a ROM image by adding header information and then concatenates the files	OSF/1, Windows NT

For your convenience, this kit includes the Free Software Foundation version of the GNU Linker (GLD).

9.2 Supported Features and Usage Requirements

The following points highlight the supported features, along with known requirements for successful usage of the software tools provided in the Alpha AXP Evaluation Board Software Tools Kit:

- GAS
  - GAS supports only a.out format and cannot be used with the OSF/1 loader.
  - There are limitations when using symbolic address constructs:
    - Label +/– a constant is supported.
    - Label +/– a label is not supported.

  * Other operators such as an asterisk (*) or a slash (/) are not supported.

- If more than one source file is used, all absolute locations need to be declared in the first source file.
- Any page alignment requirements from the first to second source file must be completed at the end of the first source file. Performing an align in a second file adds an absolute page of address space.

• PVC

- The go command in PVC causes PVC to check all the entry points described in the entry points list file generated by running ALIST with the `-e` option.
- If data is embedded in .text segments, or if files are assembled with the .data and .text merged (the `-R` option), then *all* labels for data are interpreted by ALIST as .text labels. This happens because running ALIST with the `-e` option searches the object file of symbol information about .text labels, and in the previous two cases ALIST cannot distinguish between .text and .data segment labels.

  Thus, `alist -e` can generate spurious entries that will be interpreted by PVC as PAL entry points to check. This checking will produce spurious errors.

  To avoid these errors, follow a strict naming convention and differentiate data labels from PAL entry points. If you are using the OSF/1 operating system, use `grep` to filter out unwanted, false entry points generated by `alist -e`. For example, if all of your PAL entry points were named `pal$`, use this command:

  ```
  cat pallib.ent | grep 'pal$' > pallib.ent
  ```

  Alternatively, you could assign data labels in a particular way and filter out only the labels.

  ```
  cat pallib.ent | grep -v 'data' > pallib.ent
  ```

10 Overview of DECchip 21064 and DECchip 21066 OSF/1 PALcode

PALcode is the Privileged Architecture Library code for the Alpha AXP architecture. The DECchip 21064 and DECchip 21066 OSF/1 PALcode is one design and implementation of this code. System designers can use this PALcode as a sample implementation, or customize it to create their own PALcode to support their DECchip system designs. The DECchip 21064 and DECchip 21066 OSF/1 PALcode provides a standard programming interface to the DECchip 21064 and DECchip 21066 microprocessors that

- Is tailored to the OSF/1 operating system
- Can be adapted for embedded system designs
- Can be adapted for other UNIX type operating systems

10.1 PALcode and the Alpha AXP Evaluation Board Software Developers Kit

The Alpha AXP Evaluation Board Software Developers Kit contains the PALcode source files needed to build PALcode for all Alpha AXP evaluation boards. A Makefile is also provided to control the building of the necessary objects and executable images. Pre-built objects and executable images, tailored to the OSF/1 operating system, are also provided for your convenience.

11 The Alpha AXP SROM Mini-Debugger

The SROM provides basic hardware debugging capability through a serial connector interface to the serial ROM port of the DECchip 21064 microprocessor. Using only an SROM containing this program, a clock source, a CPU chip, and a few gates, you can exercise the device connected to the CPU to debug cache, memory, and I/O subsystems until the board is functional enough to support a more fully featured monitor.

The mini-debugger provides the following:

- Basic hardware debugging capability
- A monitor that can point to hardware addresses and exercise them
- The ability to examine and deposit memory
- Support for variable baud rates and processor speeds

Refer to the *Alpha AXP SROM Mini-Debugger User's Guide* for more information about the SROM Mini-Debugger and how to initialize the EB64+.

11.1 SROM Mini-Debugger Source Files

The file `mini_dbg.hex` contains the code for the SROM Mini-Debugger. It is an executable file in the form of an Intel hex file that is ready to be programmed into a 1736A SROM or equivalent. The file does not require unpacking.

12 Registration Card

To register your evaluation board and be notified of changes, and updates, as well as new kits and products available from Digital Equipment Corporation, please complete the registration card included in the kit, or send the following information to the address listed below:

Name
Company
Address
Product purchased
Serial number
Date purchased

Mail the above information to:

Digital Equipment Corporation
Marketing/Product Updates
HLO2-2/M9
77 Reed Road
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