DECchip 21050 PCI-to-PCI Bridge Evaluation Board

User's Guide

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Preface

This guide describes the DECchip 21050 PCI-to-PCI Bridge Evaluation Board, which is an evaluation and development board for systems based on the DECchip 21050 PCI-to-PCI Bridge chip. The DECchip 21050 PCI-to-PCI Bridge Evaluation Board (also referred to as the EB50) complies with the electrical and protocol requirements of the *PCI Local Bus Specification, Revision 2.0* and the *PCI-to-PCI Bridge Architecture Specification, Revision 1.0*.

Audience

This document is for developers who are using the EB50 to design software for the DECchip 21050 PCI-to-PCI Bridge and evaluate its functionality.

Content

This guide contains the following chapters and an appendix:

- **Chapter 1, Introduction** — Describes the EB50 including the hardware requirements for using the board, secondary slot numbering, and typical configurations.
- **Chapter 2, Interrupt Forwarding and Bus Arbitration** — Describes the interrupt forwarding and secondary bus arbitration functions, and the jumpers for these operations.
- **Chapter 3, Kit Contents and Installation** — Lists the kit contents and provides the procedure for installing the EB50.
- **Appendix A, Technical Support, Ordering, and Associated Literature** — Provides information about ordering Digital's microprocessor and peripheral chips, and associated literature. It also explains how to obtain technical support.

Conventions

The following conventions are used in this guide:

Convention	Description
Notes	Provide additional information.
Signal names	Signals that connect to the DECchip 21050 PCI-to-PCI Bridge chip are defined as follows: • The leading letter indicates the source of the signal: – **s_** indicates the secondary PCI bus. – **p_** indicates the primary PCI bus. – **x** indicates that the signal is from the initiator or bus master. – **y** indicates that the signal is from the target or slave device. • The middle letters represent the signal name. • The suffix **_l** means the signal is asserted low. Signals that are asserted high have no suffix. For example, **s_trdy_l** indicates that the secondary PCI bus signal **trdy** is asserted low.
Bits	The bit of the specified bused signal is indicated in angle brackets. For example, **s_ad<21>**. A pair of numbers in the angle brackets separated by a colon (:) indicates a multiple bit field. For example, **<7:3>** specifies bits 7, 6, 5, 4, and 3.

1 Introduction

This chapter describes the DECchip 21050 PCI-to-PCI Bridge Evaluation Board (EB50) including the hardware requirements for using the board, secondary slot numbering and IDSEL mapping, and typical configurations.

1.1 DECchip 21050

The DECchip 21050 PCI-to-PCI Bridge (21050) is a low-cost, high-performance chip that expands the electrical capacity of all PCI systems (for example, Alpha AXP, PENTIUM, x86). The 21050 allows motherboard designers to add more PCI devices or more PCI option card slots than a single PCI bus can support. Option card designers can use the 21050 to implement multiple device PCI option cards.

The 21050 has two PCI interfaces. The primary PCI interface connects directly to the PCI bus closest to the host CPU. The secondary PCI interface creates a new and independent PCI bus. The primary function of the bridge is to allow transactions to occur between a master on one PCI bus and a target on the other PCI bus.

The 21050 also allows the two PCI buses to operate independently. A master and a target located on the same PCI bus can communicate with each other even if the other PCI bus is busy. As a result, the 21050 can isolate traffic between devices on one PCI bus from devices on other PCI buses. This is a major benefit to system performance in some applications such as multimedia.

For detailed information about the 21050, refer to the *DECchip 21050 PCI-to-PCI Bridge Data Sheet*.

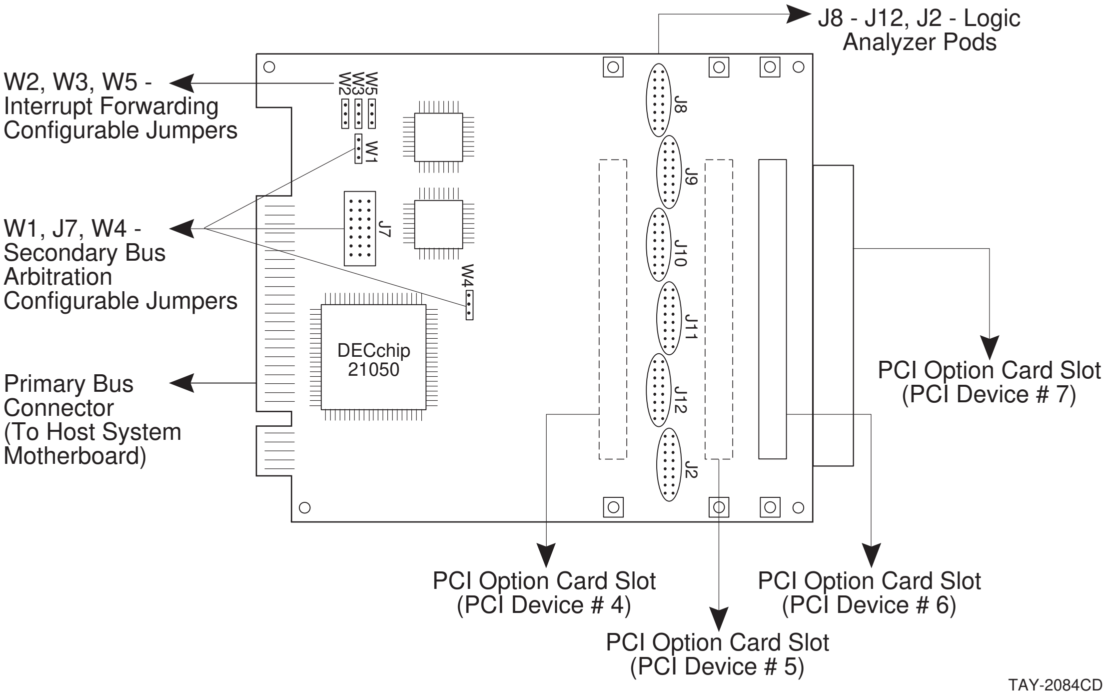
1.2 DECchip 21050 PCI-to-PCI Bridge Evaluation Board

The DECchip 21050 PCI-to-PCI Bridge Evaluation Board (EB50) is a +5-volt PCI expansion board that is used to evaluate the operation of the DECchip 21050 PCI-to-PCI Bridge in various configurations, and with a variety of PCI devices. Using the EB50, you can

- Develop initialization code to configure a PCI-to-PCI bridge and the PCI devices behind the bridge.
- Evaluate the operation of the PCI-to-PCI bridge with a variety of PCI devices attached to the secondary bus.
- Build and evaluate a flexible hierarchy for multiple PCI buses.

Figure 1–1 shows the major components on the EB50.

Figure 1–1 DECchip 21050 PCI-to-PCI Bridge Evaluation Board



1.2.1 Features

The EB50 has the following features:

- A DECchip 21050 PCI-to-PCI bridge that provides bridging between a primary and secondary bus
- A primary PCI bus that plugs into any +5-volt PCI expansion card slot
- Four secondary PCI bus expansion card slots
- Full protocol and electrical PCI revision 2.0 compliance
- Selectable external secondary bus arbiter
- Interrupt forwarding with selectable data synchronization
- Support for multiple levels of PCI bus hierarchy

1.2.2 Hardware Requirements

The following equipment is required to use the EB50:

- A computer system equipped with a PCI motherboard.
- Full compliance of the *PCI Local Bus Specification, Revision 2.0*.
- A PCI expansion slot equipped for the +5-volt environment.
- One or more PCI option cards installed in the secondary expansion bus slots. If the secondary slots are empty, only bridge initialization is supported.

1.2.3 Software Requirements

To test the EB50 in x86 DOS or windows systems, BIOS must include auto-configuration code for PCI-to-PCI bridges. If the system BIOS does not include this functionality, contact your BIOS vendor to obtain code with PCI-to-PCI bridge auto-configuration support.

1.2.4 Specifications

The physical and power specifications for the EB50 are as follows:

Dimensions:

Height: 6.90 in (17.526 cm)

Width: 5.20 in (13.208 cm)

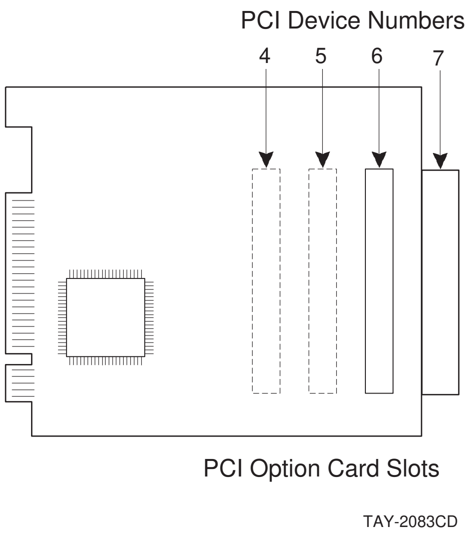
Power Requirements:

dc amps @ +5-volt: 2.0 A (maximum)

1.3 Secondary Slot Numbering and IDSEL Mapping

The PCI secondary bus expansion slots are mapped to device numbers 4, 5, 6, and 7 as shown in Figure 1–2. The secondary bus AD lines **s_ad<23:20>** are used as secondary IDSEL lines.

Figure 1–2 Secondary PCI Slot Device Numbering



1.4 Typical Configurations

The EB50 supports various PCI configurations with different types of devices. Figures 1–3 through 1–6 are sample PCI configurations.

The primary bus connector attaches to a PCI slot on the motherboard of the host system, or to a secondary PCI bus slot on another EB50. A +5-volt or universal option PCI card, or another EB50 can be plugged into any one of the four secondary bus option card slots.

Figure 1–3 DECchip 21050 PCI-to-PCI Bridge Evaluation Board with One Secondary Bus Option Card

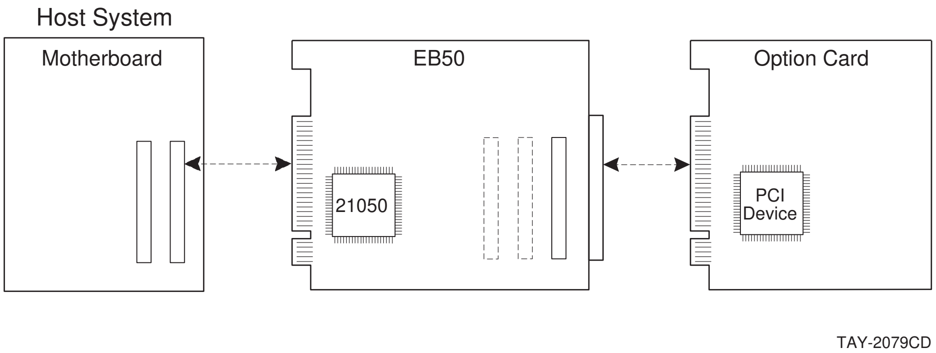


Figure 1–4 DECchip 21050 PCI-to-PCI Bridge Evaluation Board with Two Secondary Bus Option Cards

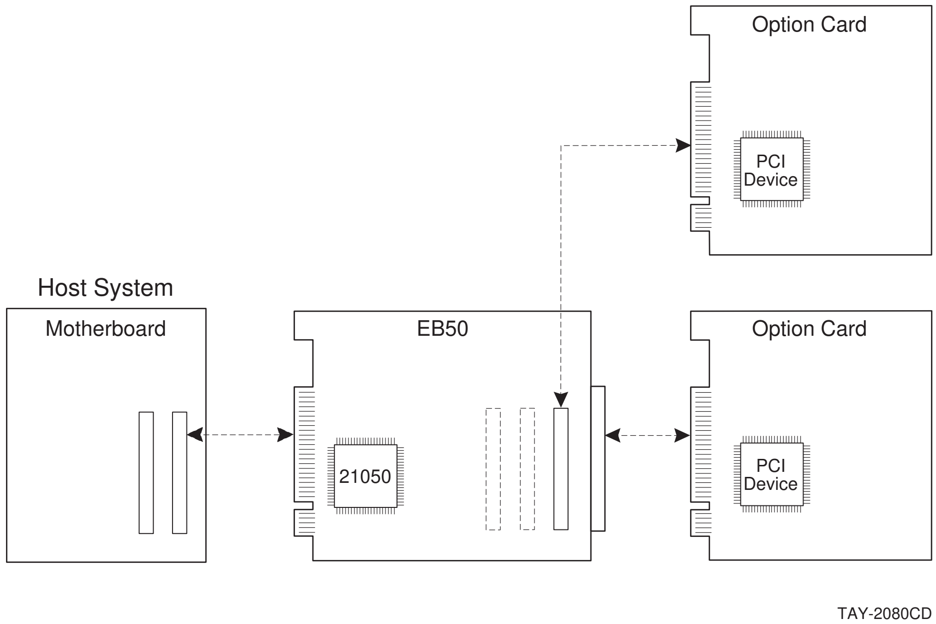


Figure 1–5 3-Level Bus with Dual DECchip 21050 PCI-to-PCI Bridge Evaluation Boards

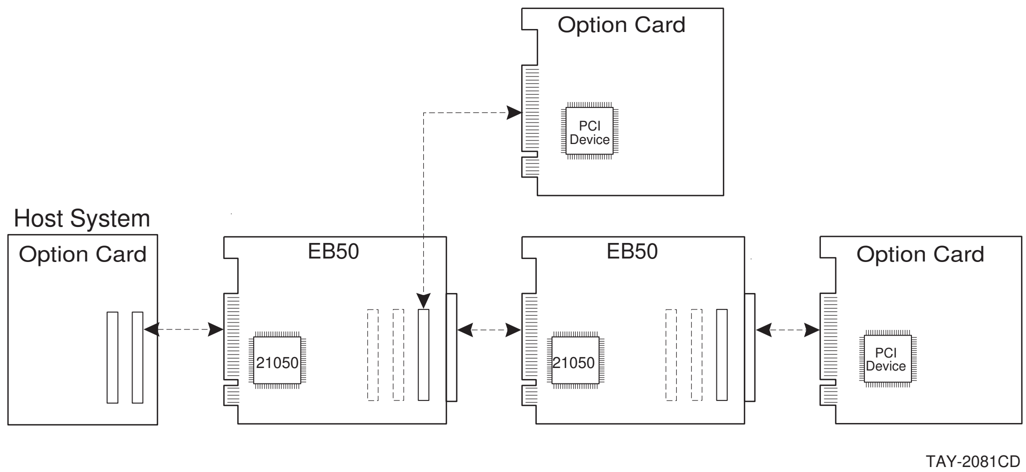
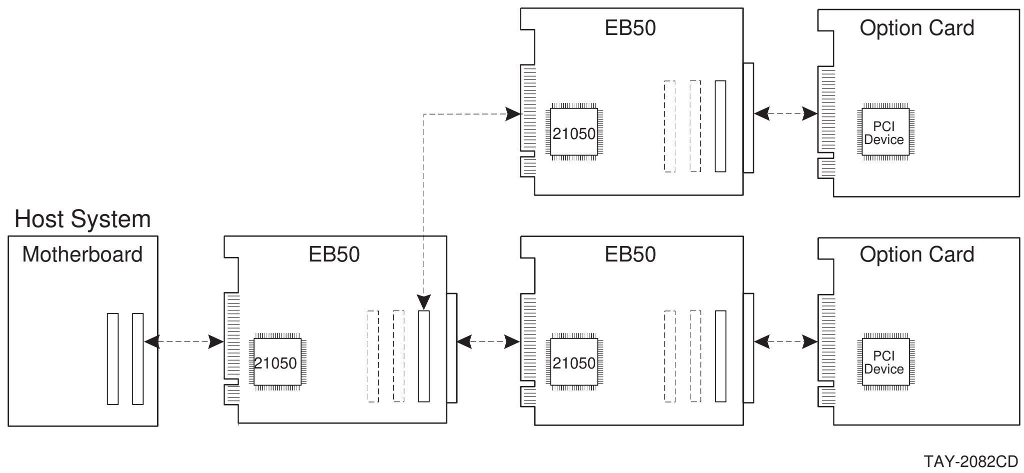


Figure 1–6 Four PCI Buses in a 3-Level Hierarchy



2

Interrupt Forwarding and Bus Arbitration

This chapter describes the interrupt forwarding and secondary bus arbitration functions, and includes information about the jumpers for these operations.

2.1 Interrupt Forwarding

A programmable array logic (PAL) on the DECchip 21050 PCI-to-PCI Bridge Evaluation Board (EB50) forwards interrupts with or without hardware data synchronization. This section describes how the PAL that is shipped with the EB50 is programmed. Other behavior may be tested by inserting a new PAL or by reprogramming the PAL with your own logic.

2.1.1 Interrupt Forwarding Synchronized with Data

The PAL forwards interrupts synchronized with data when any of the 16 secondary slot interrupt lines is low (asserted) and when posted write data is flushed. The following sequence occurs:

1. The PAL asserts (low) **s_dispst_l**.
2. **s_dispst_l** asserting (falling) edge marks posted write data in the 21050 data buffer and disables write posting (if the disable posting bit in the 21050 configuration space is set).
3. Interrupts are not forwarded until **s_bufne_l** is detected high (deasserted).

If the 21050 data buffer is not empty, the 21050 asserts (low) **s_bufne_l** two cycles after the asserting edge of **s_dispst_l**. The PAL blocks the interrupts from going to the motherboard until **s_bufne_l** is deasserted (high). As long as **s_dispst_l** is asserted and **s_bufne_l** is deasserted, the PAL forwards all interrupts.

When write posting is enabled and a second interrupt occurs before a previous interrupt clears, the second interrupt may be forwarded before the data associated with it is flushed. This occurs when **s_dispst_l** from the first interrupt stays asserted, and **s_bufne_l** reflects the write data that was posted when the first interrupt asserted.

For more information about the **s_dispst_l** and **s_bufne_l** signals, refer to the *DECchip 21050 PCI-to-PCI Bridge Data Sheet*.

2.1.2 Interrupt Forwarding Without Data Synchronization

When interrupt forwarding without data synchronization is used, the four interrupt lines from each secondary slot are simply combined and sampled by flip-flops synchronized to the secondary PCI clocks. Both the assertion and deassertion of interrupts is delayed by one PCI clock cycle through the PAL.

2.1.3 Interrupt Combining

Because a total of 16 interrupts are connected to the secondary bus PCI slots (INTA#, INTB#, INTC#, and INTD# for each slot) and only four interrupts are driven to the card edge, the 16 incoming interrupts must be combined. This ORing of interrupts is performed in accordance with the *PCI-to-PCI Bridge Architecture Specification*, and the interrupt combining is done in both synchronized and non-synchronized forwarding modes.

Table 2–1 shows the ORing of interrupts.

Table 2–1 Interrupt ORing

Device Number	Interrupt Pin on Device	Interrupt Pin on Board Connector
4	INTA#	INTA#
	INTB#	INTB#
	INTC#	INTC#
	INTD#	INTD#
5	INTA#	INTB#
	INTB#	INTC#
	INTC#	INTD#
	INTC#	INTA#
6	INTA#	INTC#
	INTB#	INTD#
	INTC#	INTA#
	INTD#	INTB#
7	INTA#	INTD#
	INTB#	INTA#
	INTC#	INTB#
	INTD#	INTC#

2.1.4 Interrupt Forwarding Jumpers

The following interrupt forwarding modes can be selected using jumpers W2, W3, and W5:

- Non-data synchronized interrupt forwarding with 21050 write posting enabled. This is the default setting.
- Non-data synchronized interrupt forwarding with 21050 write posting disabled.
- Data synchronized interrupt forwarding with PAL control of the **s_dispst_l** signal.

Figure 2–1 shows the jumper locations on the EB50. Tables 2–2 through 2–4 describe the jumper positions, and Figure 2–2 shows the settings.

All jumper positions assume that the EB50 is positioned with the components facing forward and the card edge facing down.

Figure 2–1 Jumper Locations

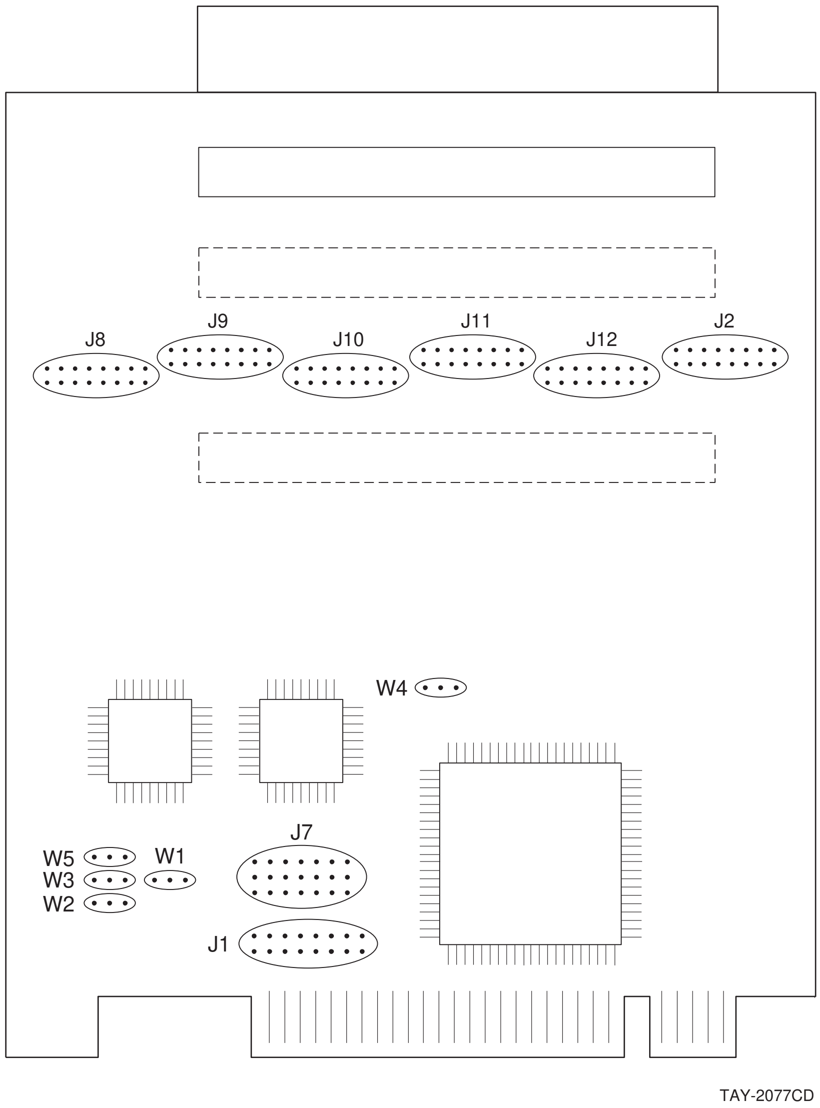


Table 2–2 Non-Data Synchronized Interrupt Forwarding with Write Posting Enabled

Jumper	Position	Description
W2	Right	Selects jumper W3, which ties **s_dispst_l** to a fixed value.
W3	Right	Selects +5-volt for **s_dispst_l** input.
W5	Right	Selects 0-volt and disables interrupt PAL data synchronization mode.

Table 2–3 Non-Data Synchronized Interrupt Forwarding with Write Posting Disabled *

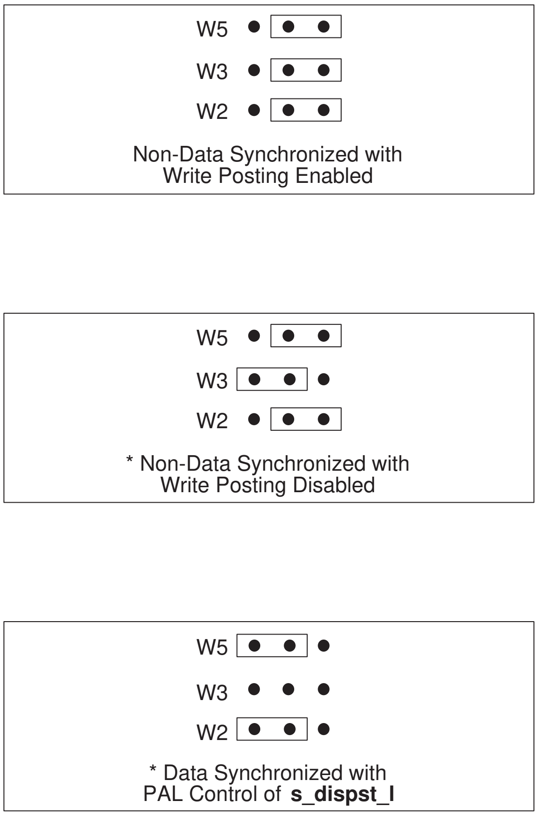
Jumper	Position	Description
W2	Right	Selects jumper W3, which ties **s_dispst_l** to a fixed value.
W3	Left	Selects 0-volt for **s_dispst_l** input.
W5	Right	Selects 0-volt and disables interrupt PAL data synchronization mode.

Table 2–4 Data Synchronized Interrupt Forwarding with PAL Control of s_dispst_l *

Jumper	Position	Description
W2	Left	Selects **s_dispst_l** control from interrupt PAL.
W3	–	Any position—jumper W3 is not selected.
W5	Left	Selects +5-volt and enables interrupt PAL data synchronization mode.

* For this configuration, the posting bit in the 21050 configuration space must be set to disable posting. For more information, refer to the *DECchip 21050 PCI-to-PCI Bridge Data Sheet*.

Figure 2–2 Interrupt Forwarding Jumper Settings



* For this configuration, the posting bit in the 21050 configuration space must be set to disable posting. For more information, refer to the *DECchip 21050 PCI-to-PCI Bridge Data Sheet.*

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2.2 Secondary Bus Arbitration

The EB50 has two secondary bus arbiter systems — an internal arbiter implemented in the 21050 and an external arbiter implemented in an AMD MACH210A programmable device. The internal 21050 arbiter can be configured to operate in rotating or modified rotating mode. In modified rotating mode, the bridge is given highest priority on alternate transactions. Secondary bus parking is done by default at the 21050.

The external arbiter system resides in the PAL and implements straight-rotating arbitration. Secondary bus parking is done at the 21050. If a different external arbiter is used where parking is done at one of the PCI slots, a PCI device must be installed in that slot.

The default setting is internal arbitration. To change the default, refer to the jumper information in the next section.

2.2.1 Bus Arbitration Jumpers

To configure the secondary bus arbiter system, use jumpers J7, W4, and W1. All jumper positions assume that the EB50 is positioned with the components facing forward and the card edge facing down. See Figure 2–1 for the jumper locations. Tables 2–6 and 2–5 describe the jumper positions, and Figure 2–3 shows the settings.

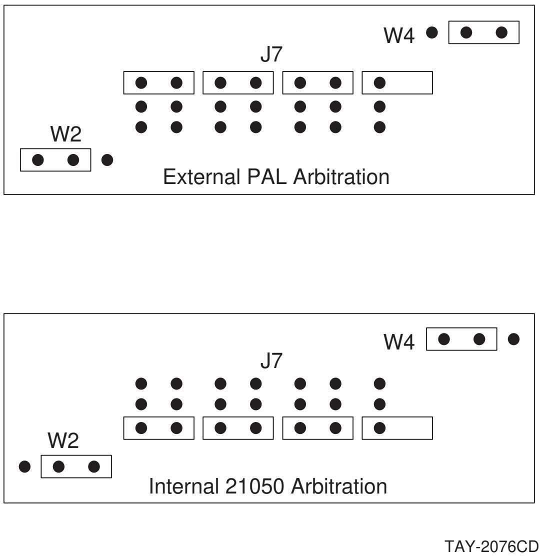
Table 2–5 External PAL Arbitration

Jumper	Position	Description
J7	Top	Selects the PAL as the source of secondary grants.
W4	Right	Selects the board signals **gt_out<4>** (the external secondary grant to the 21050) to drive the bridge **s_req_l<0>** input.
W1	Left	Ties **s_cfn_l** high, which disables the internal 21050 arbiter and causes the following reconfigurations: • **s_gnt_l<0>** becomes the secondary bus request • **s_req_l<0>** becomes the secondary bus grant The PAL parks the secondary bus at the 21050.

Table 2–6 Internal 21050 Arbitration

Jumper	Position	Description
J7	Bottom	Selects the 21050 as the source of secondary grant signals.
W4	Left	Selects the board signal **sreq<0>l** (device 4 request signal) to drive the bridge **s_req_l<0>** input.
W1	Right	Ties **s_cfn_l** low, which enables the 21050 internal arbiter. When the secondary PCI bus is idle, parking is at the bridge.

Figure 2–3 Secondary Bus Arbitration Jumper Settings



3
Kit Contents and Installation

This chapter lists the contents of the DECchip 21050 PCI-to-PCI Bridge Evaluation Board Kit, and describes how to install the DECchip 21050 PCI-to-PCI Bridge Evaluation Board.

3.1 Kit Contents

The DECchip 21050 PCI-to-PCI Bridge Evaluation Board Kit contains the following materials. If any items are missing or damaged, contact your Digital sales representative.

- DECchip 21050 PCI-to-PCI Bridge Evaluation Board (EB50)
- A documentation package that includes the following:
  - *DECchip 21050 PCI-to-PCI Bridge Data Sheet*
  - *DECchip 21050 PCI-to-PCI Bridge Product Brief*
  - *DECchip 21050 PCI-PCI Bridge Configuration: An Application Note*
  - *DECchip 21050 PCI-PCI Bridge Hardware Implementation: An Application Note*
  - *DECchip 21050 Evaluation Board Vendor Parts List*
  - *DECchip 21050 PCI Evaluation Board Schematics (MD and UA)*
  - Warranty agreement/registration card

3.2 Installation Procedure

To install the EB50, do the following:

1. If necessary, reconfigure the interrupt forwarding and secondary bus arbitration jumpers. The default settings are non-data synchronized interrupt forwarding with write posting enabled, and internal 21050 bus arbitration.

   To change a default setting, refer to the jumper information in Chapter 2. Then, return to this procedure.

2. Power down the PCI slot on the motherboard of the host system that will contain the EB50.

3. Place the motherboard with the associated support devices on a bench. This is necessary because mechanical constraints may not allow testing of the EB50 and expansion slots inside the system box.

4. Insert the card edge of the EB50 into the powered down PCI slot.

5. Plug a +5-volt or universal option PCI card, or another EB50 into any one or more of the four secondary bus option card slots. The **Typical Configurations** section in Chapter 2 shows sample PCI configurations.

6. Power on the PCI slot containing the EB50.

7. Test auto-configuration and device operation as follows:

   - Make sure the BIOS or firmware detects and configures the PCI devices downstream of the 21050.

   - Install the device driver for the PCI devices downstream of the 21050, and make sure that the device operates correctly.

8. If desired, monitor the secondary PCI signals of the bridge by connecting a logic analyzer to jumpers J2 and J8 through J12.

A

Technical Support, Ordering, and Associated Literature

This appendix provides information about ordering Digital's microprocessor and peripheral chips, and associated literature. It also explains how to obtain technical support and information.

A.1 Semiconductor Information Line

Use the following numbers to call the Semiconductor Information Line for information and technical support:

United States and Canada	**1–800–332–2717**
TTY (United States only)	**1–800–332–2515**
Outside North America	**+1–508–568–6868**

A.2 Ordering DECchip Products

To order the following DECchip products, contact your local Digital sales office. Your sales representative may be able to help you take advantage of discounts and volume pricing.

Product	Order Number
DECchip 21050 PCI-to-PCI Bridge	21050–AA

A.3 Ordering Associated DECchip Literature

The following table lists DECchip 21050 literature that is available. For order information, contact the Semiconductor Information Line.

Title	Order Number
DECchip 21050 PCI-to-PCI Bridge Product Brief	EC–Q9Y0A-TE
DECchip 21050 PCI-to-PCI Bridge Data Sheet	EC–Q9XVA-TE
DECchip 21050 PCI-PCI Bridge Configuration: An Application Note	EC–Q9Y4A-TE
DECchip 21050 PCI-PCI Bridge Hardware Implementation: An Application Note	EC–Q9Y3A-TE

A.4 Ordering Third-Party Literature

You can order the following third-party literature directly from the vendor.

Title	Vendor
PCI Local Bus Specification PCI-to-PCI Bridge Architecture Specification	PCI Special Interest Group M/S HF3–15A 5200 N.E. Elam Young Pkwy Hillsboro, Oregon 97124–6497 (503) 696–2000