DECchip 21040
Ethernet LAN Controller for PCI

Data Sheet

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1 DECchip 21040 Overview

The DECchip 21040 Ethernet LAN Controller (21040) supports the peripheral controller interconnect (PCI) bus. It provides a glueless connection to the PCI and adapts easily to most other standard buses. The 21040 provides a direct Ethernet connection to the twisted-pair (TP) interface and attachment unit interface (AUI).

1.1 General Description

The 21040 interfaces with the PCI using on-chip control and status registers (CSRs), and a shared PCI memory area that is set up mainly during initialization. This minimizes the processor involvement in the 21040 operation during normal reception and transmission. The 21040 is PCI Revision 2.0-compliant. Bus traffic is also minimized by filtering out received runt frames and by automatically retransmitting collided frames without needing to repeat a fetch from PCI memory.

On the network side, the 21040 provides an AUI and a twisted-pair interface, enabling a low chip count connection to the two most popular Ethernet interfaces. The 21040 can sustain transmission or reception of minimal-sized back-to-back packets at full line speed with an interpacket gap (IPG) of 9.6 microseconds. It is also capable of functioning in a full-duplex environment.

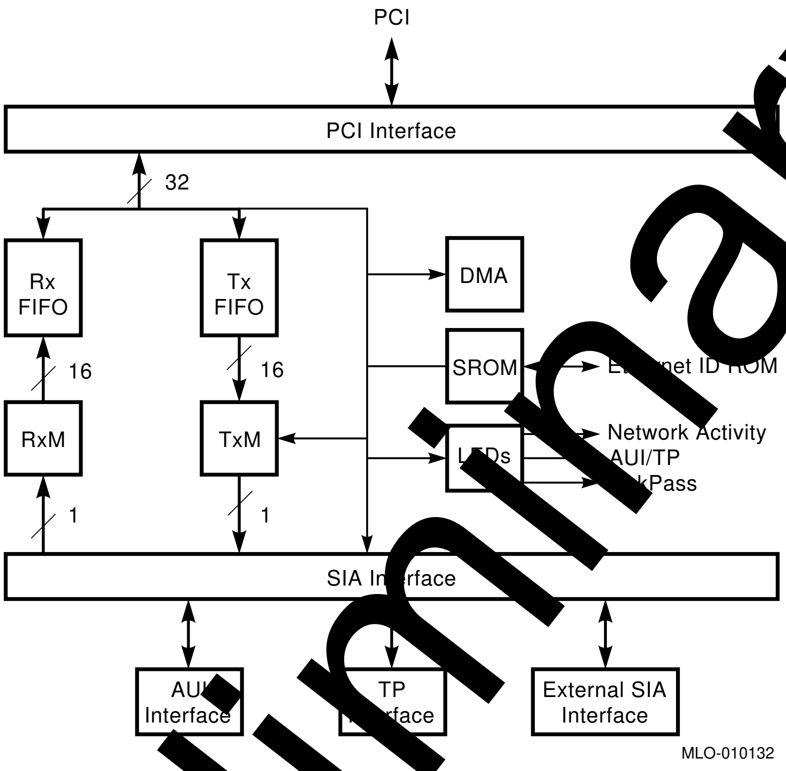
1.2 DECchip 21040 Microarchitecture

The following list describes the microarchitecture components, and Figure 1 shows the 21040 microarchitecture.

- PCI interface—Includes all interface functions to the PCI bus; handles all interconnect control signals; executes PCI direct-memory access (DMA) and I/O transactions.
- DMA—Dual receive and transmit controller; supports bursts of up to 32 longwords; handles data transfers between PCI memory and on-chip memory.
- FIFOs—Dual 256-byte FIFOs for receive and transmit; supports automatic packet deletion (runt packets or after a collision) and packet retransmission after a collision on transmit.
- TxM—Handles all CSMA/CD[1] MAC[2]-level transmit operations and transfers data from transmit FIFO to the serial interface attachment (SIA) for transmission.
- RxM—Handles all CSMA/CD receive operations and transfers the data from the SIA to the receive FIFO.
- SIA—Performs physical layer operations; implements the AUI and 10BASE-T functions, including the Manchester encoder and decoder functions.

[1] Carrier-sense multiple access with collision detection
[2] Media access control

Figure 1   DECchip 21040 Microarchitecture



1.3 Features

The 21040 has the following features:

- Offers a single-chip Ethernet controller for PCI local bus
  - Provides glueless connection to PCI bus
  - Contains on-chip integrated attachment unit interface (AUI) port and a 10BASE-T transceiver
- Supports full-duplex operation
- Provides clock speed up to 33 megahertz, with no wait states on PCI master operation
- Enables powerful on-chip DMA with programmable, unlimited burst size providing for low CPU utilization
- Implements unique, patent-pending intelligent arbitration between DMA channels preventing underflow or overflow and optimized for full-duplex
- Contains two large (256-byte) independent receive and transmit FIFOs
- Supports either big or little endian byte ordering
- Implements JTAG-compatible test access port with boundary-scan pins
- Provides full support of IEEE 802.3, ANSI 8802-3, and Ethernet standards
- Offers a unique, patented solution to Ethernet capture effect problem
- Contains a variety of flexible address filtering modes
  - 16 perfect addresses or
  - 512 hash-filtered multicast addresses and one perfect address or
  - 512 hash-filtered physical addresses and multicast addresses
  - Inverse perfect filtering
- Provides serial ROM interface for Ethernet ID address ROM
- Supports three LEDs: network activity, LinkPass, and AUI/10BASE-T
- Enables automatic detection and correction of 10BASE-T receive polarity
- Provides external and internal loopback capability
- Implements low power, 3.3 V complimentary metal oxide semiconductor (CMOS) device, interfaces to 5.0 V or 3.3 V logic

2 Pinout

The tables in this section provide a description of the pins and their respective signal definitions. Table 1 lists the tables in this section.

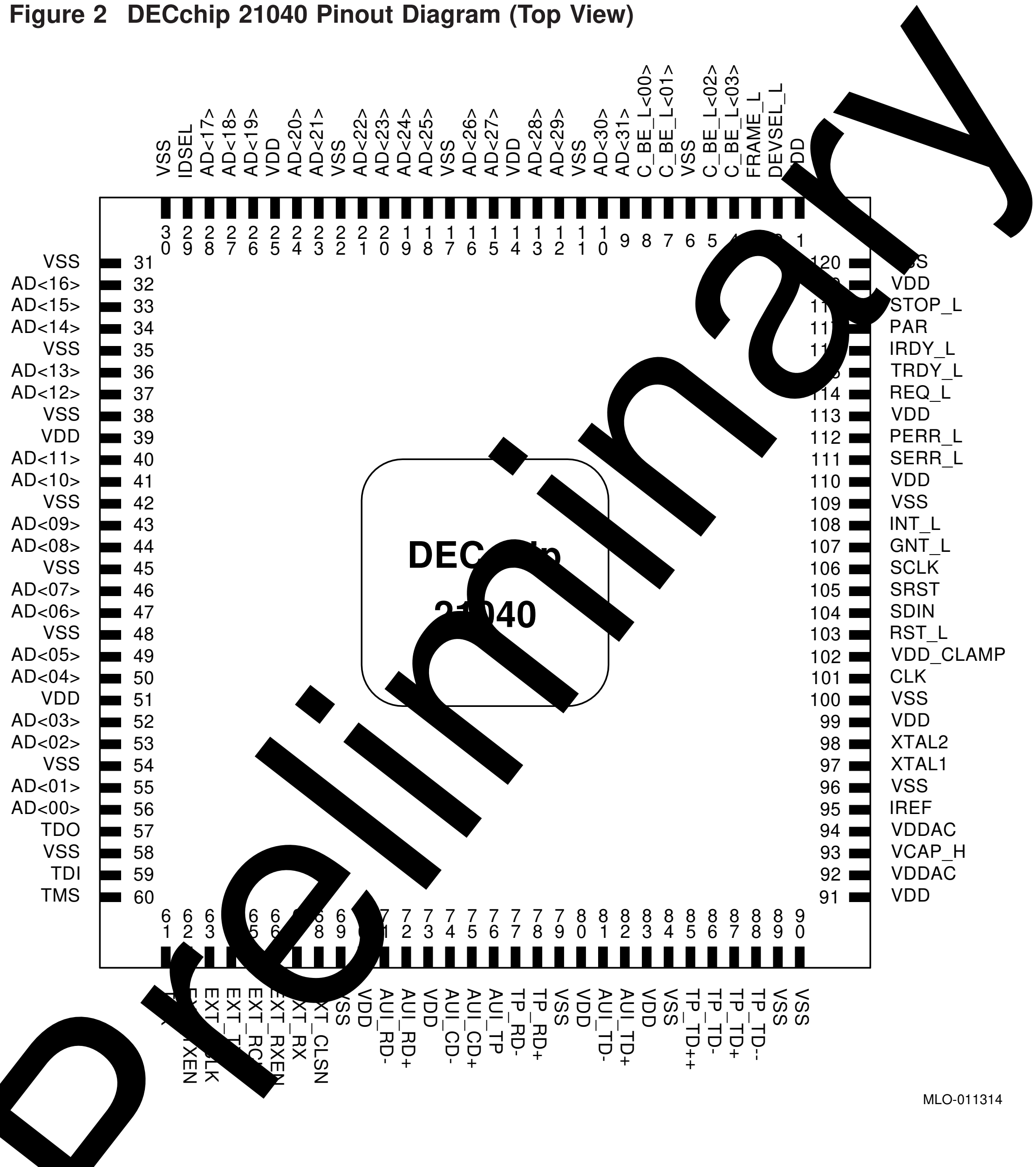
Table 1 Index to Pinout Tables

For this information . . .	Refer to . . .
Pin cross reference by logic signal	Table 2
Pin cross reference by power signal	Table 3
Quick pin reference	Table 4
Input pin reference	Table 5
Output pin reference	Table 6
Input/output pin reference	Table 7
Signal functions	Table 8

2.1 Pinout and Pin Descriptions

The 21040 is housed in the 120-pin plastic quad flat pack. The 21040 uses all pins. Figure 2 shows the 21040 pinout.

Figure 2 DECchip 21040 Pinout Diagram (Top View)



2.2 Quick Pin Reference

Table 2 provides a pin cross reference listed by logic signal name. Table 3 provides a pin cross reference listed by power signal name. Table 4 is a quick pin reference that defines the logic signals.

Table 2 DECchip 21040 Pin Cross Reference by Logic Signal

Signal	Location	Signal	Location
AD[00]	56	AD[28]	13
AD[01]	55	AD[29]	12
AD[02]	53	AD[30]	10
AD[03]	52	AD[31]	9
AD[04]	50	AUI_CD–	74
AD[05]	49	AUI_CD+	75
AD[06]	47	AUI_RD–	71
AD[07]	46	AUI_RD+	72
AD[08]	44	AUI_TD–	81
AD[09]	43	AUI_TD+	82
AD[10]	41	AUI_TP	76
AD[11]	40	C_BE_L[00]	8
AD[12]	37	C_BE_L[01]	7
AD[13]	36	C_BE_L[02]	5
AD[14]	34	C_BE_L[03]	4
AD[15]	33	CLK	101
AD[16]	32	DEVSEL_L	2
AD[17]	28	EXT_CLSN	68
AD[18]	27	EXT_RCLK	65
AD[19]	26	EXT_RX	67
AD[20]	24	EXT_RXEN	66
AD[21]	23	EXT_TCLK	63
AD[22]	21	EXT_TX	64
AD[23]	20	EXT_TXEN	62

(continued on next page)

Table 2 (Cont.) DECchip 21040 Pin Cross Reference by Logic Signal

Signal	Location	Signal	Location
AD[24]	19	FRAME_L	3
AD[25]	18	GNT_L	107
AD[26]	16	IDSEL	29
AD[27]	15	INT_L	108
IRDY_L	116		
IREF	95	TMS	60
PAR	117	TP_RD–	77
PERR_L	112	TP_RD+	78
REQ_L	114	TP_TD–	86
RST_L	103	TP_TD– –	88
SCLK	106	TP_TD+	87
SDIN	104	TP_TD+ +	85
SERR_L	111	TRDY_L	115
SRST	105		
STOP_L	118	VCAP_H	93
TCK	61	XTAL1	97
TDI	59	XTAL2	98
TDO	57		

Table 3 DECchip 21040 Pin Cross Reference by Power Signal

Signal	Location	Signal	Location
VDD (3.3 V)	1, 14, 25	VSS (GND)	6, 11, 17, 22
	39, 51, 70, 73		30, 31, 35, 38
	80, 83, 91, 99		42, 45, 48, 54
	110, 113, 119		58, 69, 79, 84
VDD_CLAMP	102		89, 90, 96, 100,
VDDAC (3.3 V)	92, 94		109, 120

Table 4 lists a functional description of each of the 21040 signals. These signals are listed alphabetically. The functional grouping of each pin is listed in Section 2.4.

The following terms describe the 21040 pinout.

- **Address phase**

  The address and appropriate bus command are driven during this cycle.

- **Data phase**

  Data and the appropriate byte enable code are driven during this cycle.

- **_L**

  All pin names with the _L suffix are only asserted low.

Note

The following list describes the abbreviations used in the tables in this section.

I = Input
O = Output
I/O = Input/output
O/D = Open drain

Table 4 Quick Pin Reference

Signal	Type	Description
AD[31:00]	I/O	32-bit multiplexed PCI address and data lines. Address and data bits are multiplexed on the same pins. During the first clock cycle of a transaction, AD[31:00] contain a physical byte address (32 bits). During subsequent clock cycles, AD[31:00] contain data. A 21040 bus transaction consists of an address phase followed by one or more data phases. The 21040 supports both read and write bursts. Little and big endian byte ordering can be used.
AUI_CD–	I	Attachment unit interface receive collision differential negative data.
AUI_CD+	I	Attachment unit interface receive collision differential positive data.
AUI_RD–	I	Attachment unit interface receive differential negative data.
AUI_RD+	I	Attachment unit interface receive differential positive data.
AUI_TD–	O	Attachment unit interface transmit differential negative data.
AUI_TD+	O	Attachment unit interface transmit differential positive data.
AUI_TP	I	Attachment unit interface and twisted-pair select line. When asserted high, the attachment unit interface is selected. When asserted low, the twisted-pair interface is selected.
C_BE_L[03:00]	I/O	Bits 0 through 3 of the bus command and byte enable lines. Bus command and byte enable are multiplexed on the same PCI pins. During the address phase of the transaction, C_BE_L[03:00] provide the bus command. During the data phase, C_BE_L[03:00] provide the byte enable. The byte enable determines which byte lines carry valid data. For example, C_BE_L[00] applies to byte 0, and C_BE_L[03] applies to byte 3. In all initiator and I/O operations, C_BE_L[03:00] contain a value equal to a longword hexadecimal value of 0. In configuration operations, C_BE_L[03:00] can contain any value; 21040 supports byte, word, and longword operations.

(continued on next page)

Table 4 (Cont.) Quick Pin Reference

Signal	Type	Description
CLK	I	The clock provides the timing for the 21040-related bus transactions. All the other bus signals are sampled on the rising edge of CLK. The clock range is between 16 megahertz and 33 megahertz.
DEVSEL_L	I/O	Device select is asserted when it is the target of the current bus access. When the 21040 is the initiator of the current bus access, it expects the target to assert DEVSEL_L within 5 bus cycles, confirming the access. To accomplish this, the 21040 asserts this signal in a medium speed (within two bus cycles). If the target does not assert DEVSEL_L within the required bus cycles, then the 21040 aborts the cycle.
EXT_CLSN	I/O	Collision detect or test signals a collision occurrence on the Ethernet cable to the 21040. It may be asserted and deasserted asynchronously to the receive clock by the external SIA. This signal is an output to the AUI/TP LED. The LED is on when AUI is selected. This pin can be used for SIA testing features.
EXT_RCLK	I/O	Receive clock or test pin carries the recovered receive clock supplied by an external SIA. During idle periods, the RCLK pin may be inactive. This pin can be used for SIA testing features.
EXT_RX	I/O	Receive data or test pin carries the input receive data from the external SIA. The incoming data should be synchronous with the RCLK signal. This pin also outputs to the LinkPass LED. In 10BASE-T mode, when LinkPass is detected, the LED is asserted for a period of at least 300 milliseconds. In AUI mode, if CSR12 bit 1 is asserted indicating no carrier, the LED is deasserted for a period of 300 milliseconds. This pin can be used for SIA testing features.

(continued on next page)

Table 4 (Cont.) Quick Pin Reference

Signal	Type	Description
EXT_RXEN	I/O	Receive enable or test pin signals activity on the Ethernet cable to the 21040. It is asserted when receive data is present on the Ethernet cable and deasserted at the end of a frame. It may be asserted and deasserted asynchronously to the receive clock (RCLK) by the external SIA. This pin also interfaces with the network activity LED. When any activity is detected on the network, the LED is asserted for a period of at least 100 milliseconds. This pin can be used for SIA testing features.
EXT_TCLK	I/O	Transmit clock or test pin carries the transmit clock supplied by an external SIA. The clock must always be active. This pin can be used for SIA testing features.
EXT_TX	I/O	Transmit data or test pin carries the serial output data from the 21040. This data is synchronized to the TCLK signal. This pin can be used for SIA testing features.
EXT_TXEN	I/O	Transmit enable or test pin signals the 21040 transmit-in-progress to an external SIA. The pin is also used for SIA testing features. This pin can be used for SIA testing features.
FRAME_L	I/O	Cycle frame is driven by the 21040 (bus initiator) to indicate the beginning and duration of an access. When FRAME_L asserts, it indicates the beginning of a bus transaction. While FRAME_L is asserted, data transfers continue. When FRAME_L is deasserted, it indicates that the next data phase is the final data phase transaction.
GNT_L	I	Bus grant asserts to indicate to the 21040 that access to the bus is granted.
IDSEL	I	Initialization device select asserts to act as a chip select during configuration read or write transactions.

(continued on next page)

Table 4 (Cont.) Quick Pin Reference

Signal	Type	Description
INT_L	O/D	Interrupt request asserts when one of the appropriate bits of CSR5 sets and causes an interrupt, provided that the corresponding mask bit in CSR7 is not asserted. INT_L deasserts by writing a 1 into the appropriate CSR5 bit. If more than one interrupt bit is asserted in CSR5, then the host clears only the interrupt bit that was acknowledged, INT_L deasserts for one cycle and then asserts again. This process continues until all interrupts are acknowledged. When deasserted, this pin should be pulled up by an external resistor.
IRDY_L	I/O	Initiator ready indicates the bus initiator's ability to complete the current data phase of the transaction. A data phase is completed on any clock when both IRDY_L and target ready (TRDY_L) are asserted. Wait cycles are inserted until both IRDY_L and TRDY_L are asserted together. When the 21040 is the bus initiator, IRDY_L is asserted during write operations to indicate that valid data is present on AD[31:00]. During read operations, the 21040 asserts IRDY_L to indicate that it is ready to accept data.
IREF	I	Current reference input for the analog phase lock loop logic.
PAR	I/O	Parity is calculated by the 21040 as an even parity bit for the AD[31:00] and C_BE_L[03:00] lines. During address and data phases, PAR is calculated on all the AD and C_BE_L lines whether or not any of these lines carry meaningful information.
PERR_L	I/O	Parity error asserts when a data parity error is detected. When the 21040 is the bus initiator and a parity error is detected, the 21040 asserts both CSR5 bit 13 (system error) and CFCS bit 9 (SERR_L enable) and completes the current data burst transaction, then stops its operation. After the host clears the system error, the 21040 continues its operation. When the 21040 is the bus target and a parity error is detected, the 21040 asserts PERR_L.

(continued on next page)

Table 4 (Cont.)   Quick Pin Reference

Signal	Type	Description
REQ_L	O	Bus request is asserted by the 21040 to indicate to the bus arbiter that it wants to use the bus.
RST_L	I	Resets the 21040 to its initial state. This signal must be asserted for at least 10 active PCI clock cycles. When in the reset state, all output pins are put into tristate and all open drain (O/D) signals are floated.
SCLK	O	Ethernet address ROM clock is used to clock data information into the 21040.
SDIN	I	Ethernet address ROM data in is used to serially shift the Ethernet identification address from the serial ROM device into the 21040.
SERR_L	O/D	If an address parity error is detected and CFCS bit 31 (detected parity error) is enabled, then 21040 asserts both SERR_L (system error) and CFCS bit 30 (signal system error). When an address parity error is detected, system error asserts two clocks after the failing address. When deasserted, this pin should be pulled up by an external resistor.
SRST	O	Ethernet address ROM reset provides an asynchronous initialization of the serial ROM device.
STOP_L	I/O	Stop indicator indicates that the current target is requesting the bus initiator to stop the current transaction. The 21040 responds to the assertion of STOP_L when it is the bus initiator, either to disconnect, retry, or abort.
TCK	I	JTAG clock shifts state information and test data into and out of the 21040 during JTAG test operations.
TDI	I	JTAG data in is used to serially shift test data and instructions into the 21040 during JTAG test operations.
TDO	O	JTAG data out pin is used to serially shift test data and instructions out of the 21040 during JTAG test operations.
TMS	I	JTAG test mode select controls the state operation of JTAG testing in the 21040.
TP_RD–	I	Twisted-pair negative differential receive data from the twisted-pair lines.

(continued on next page)

Table 4 (Cont.) Quick Pin Reference

Signal	Type	Description
TP_RD+	I	Twisted-pair positive differential receive data from the twisted-pair lines.
TP_TD– TP_TD– –	O	Twisted-pair negative differential transmit data. The positive and negative differential transmit data outputs are resistively combined outside the 21040 with equalization to compensate for intersymbol interference on the twisted-pair medium.
TP_TD+ TP_TD+ +	O	Twisted-pair positive differential transmit data. The positive and negative differential transmit data outputs are resistively combined outside the 21040 with equalization to compensate for intersymbol interference on the twisted-pair medium.
TRDY_L	I/O	Target ready indicates the target agent's ability to complete the current data phase of the transaction. A data phase is completed on any clock when both TRDY_L and initiator ready (IRDY_L) are asserted. Wait cycles are inserted until both IRDY_L and TRDY_L are asserted together. When the 21040 is the bus initiator, TRDY_L is asserted by the bus target on the read operation indicating that valid data is present on AD[31:00]. During a write cycle, it indicates that the target is prepared to accept data.
VCAP_H	I	Capacitor input for analog phase lock loop logic.
VDD	I	3.3-volt supply input voltage.
VDDAC	I	3.3-volt supply input for analog phase lock loop logic.
VDD_CLAMP	I	Supplies +5 volts or +3.3 volts reference for the clamp logic.
VSS	—	Ground pin.
XTAL1	I	Crystal oscillator input.
XTAL2	O	Crystal feedback output pin used for crystal connections only. If this pin is unused, then do not connect it.

2.3 Pin Reference Tables

There are three pin reference tables:

- Table 5 lists the input pins.
- Table 6 lists the output pins.
- Table 7 lists the input/output pins.

Table 5 Input Pin Reference

Signal	Active Level	Signal	Active Level
AUI_CD–	Low	TCK	High
AUI_CD+	High	TDI	High
AUI_RD–	Low	TMS	High
AUI_RD+	High	TP_RD–	Low
AUI_TP	High = AUI Low = TP	TP_RD+	High
CLK	Not applicable	VCAP_H	High
GNT_L	Low	VDD	High
IDSEL	High	VDDAC	High
IREF	High	VDD_CLAMP	High
RST_L	Low	XTAL1	High
SCLK	High		
SDIN	High		

Table 6 Output Pin Reference

Signal	Active Level	Signal	Active Level
AUI_TD–	Low	TP_TD–	Low
AUI_TD+	High	TP_TD– –	Low
INT_L	Low	TP_TD+	High
REQ_L	Low	TP_TD+ +	High
SRST	High	XTAL2	High
TDO	Not applicable		

Table 7 Input/Output Pin Reference

Signal	Active Level	Signal	Active Level
AD[31:00]	Not applicable	EXT_TXEN	High
C_BE_L[03:00]	Low	FRAME_L	Low
DEVSEL_L	Low	IRDY_L	Low
EXT_CLSN	High	PAR	Not applicable
EXT_RCLK	High	PERR_L	Low
EXT_RX	High	SERR_L	Low
EXT_RXEN	High	STOP_L	Low
EXT_TCLK	High	TRDY_L	Low
EXT_TX	High		

2.4 Signal Grouping by Function

Table 8 lists the signals according to their interface function.

Table 8 Signal Functions

Interface	Function	Signal
PCI	Address and data	AD[31:00], FRAME_L, PAR
	Arbitration	GNT_L, REQ_L
	Bus command and byte enable	C_BE_L[03:00]
	Device select	DEVSEL_L, IDSEL, IRDY_L, TRDY_L
	Error reporting	PERR_L, SERR_L
	Interrupt	INT_L
	System	CLK, RST_L
Network connection	Analog phase lock loop logic	IREF, VCAP_H, VDDAC
	AUI collision data	AUI_CD–, AUI_CD+
	AUI/TP select	AUI_TP
	AUI transmit and receive data	AUI_RD–, AUI_RD+, AUI_TD–, AUI_TD+
	Crystal oscillator	XTAL1, XTAL2
	External collision detect/test	EXT_CLSN
	External receive control	EXT_RCLK, EXT_RX, EXT_RXEN
	External transmit control	EXT_TCLK, EXT_TX, EXT_TXEN
	Twisted-pair transmit and receive data	TP_RD–, TP_RD+, TP_TD–, TP_TD– –, TP_TD+, TP_TD+ +
Power and diagnostic	3.3-volt and 5-volt supply input	VDD, VDDAC, VDD_CLAMP
	Ground	VSS
Test access port	JTAG test operations	TCK, TDI, TDO, TMS
Ethernet ID port	Address ROM	SCLK, SDIN, SRST

3 Electrical and Environmental Specifications

This section contains the electrical and environmental specifications of the 21040. The test conditions for the specified values are as follows unless otherwise indicated:

- Temperature (Ta): 70°C
- Power supply voltage (VDD): 3.3 V
- Power supply voltage (VDDAC): 3.3 V
- Reference voltage (VDD_CLAMP): 3.3 V or 5.0 V
- Ground (VSS): 0 V

3.1 Voltage Limit Ratings

Table 9 lists the voltage limit ratings.

Table 9 Voltage Limit Ratings

Parameter	Minimum	Maximum
Power supply voltage	+3.135 V	+3.465 V
VDD_CLAMP (5.0 V)	+4.75 V	+5.25 V
VDD_CLAMP (3.3 V)	+3.135 V	+3.465 V
ESD protection voltage	–	2000 V

Caution

Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21040. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21040.

3.2 Temperature Limit Ratings

Table 10 lists the temperature limit ratings.

Table 10 Temperature Limit Ratings

Parameter	Minimum	Maximum
Storage temperature	–55°C	+125°C
Operating temperature	0°C	70°C

Caution

Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21040. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21040.

3.3 Supply Current and Power Dissipation

The values in Table 11 are estimates based on a PCI clock frequency of 33 megahertz and a network clock frequency of 10 megahertz.

Table 11 Supply Current and Power Dissipation

Symbol	Conditions	Typical	Maximum	Units
IDD	VDD=3.465 V, Ta =70 C	160	210	mA
Power	VDD=3.465 V, Ta=70 C	0.52	0.72	Watts

3.4 PCI Bus Electrical Specifications

This section contains information about electrical characteristics for the 21040 PCI.

3.4.1 PCI I/O Voltage Specifications

The 21040 meets the I/O voltage specifications listed in Table 12.

Table 12 I/O Voltage Specifications for 5.0-Volt Levels

Category	PCI I/O	PCI Output	PCI Input
Vil	O.8 V	Not applicable	0.8 V
Vih	2.0 V	Not applicable	2.0 V
Vol[1]	0.55 V	0.55 V	Not applicable
Voh	2.4 V	2.4 V	Not applicable
Ioh	–2 mA	–2 mA	Not applicable
Ioz	+/–10 µA	+/–10 µA	Not applicable
Max Vin	5.6 V	Not applicable	5.6 V
Cap[2]	8 pF	8 pF	8 pF

[1] Signals without pullup resistors must have 3 milliamps low output current. Signals requiring pullup resistors (including **frame_l, trdy_l, irdy_l, devsel_l, stop_l, serr_l, and perr_l**) must have 6 milliamps.

[2] Parameter design guarantee.

3.4.2 PCI Reset

PCI reset (RST) is an asynchronous signal that must be active for at least 10 PCI CLK cycles. Figure 3 shows the PCI reset timing characteristics, and Table 13 lists the PCI reset signal limits.

Figure 3 PCI Reset Timing Diagram

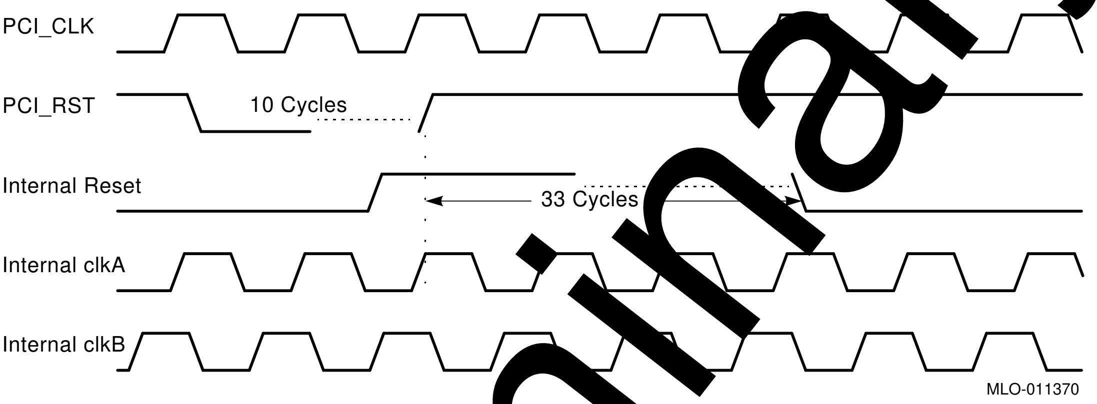


Table 13 PCI Reset Timing

Symbol	Parameter	Minimum	Maximum	Notes
Trst	RST pulse width	10*Tcycle	Not applicable	CLK active

3.4.3 PCI Clock Specifications

The standard clock frequency range for the PCI is between 16 megahertz and 33 megahertz. Figure 4 shows the PCI clock specification timing characteristics, and Table 14 lists the frequency-derived clock specifications.

Figure 4 PCI Clock Specifications Timing Diagram

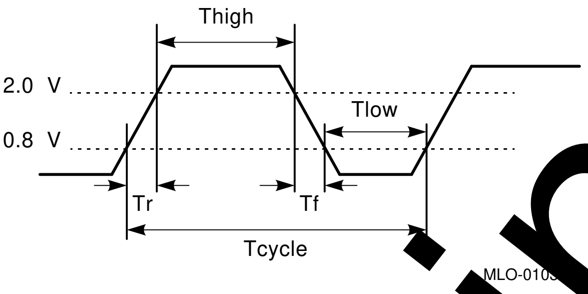


Table 14 PCI Clock Specifications

Symbol	Parameter	Minimum	Maximum	Notes
Tcycle	Cycle time	30 ns	62.5 ns	–
Thigh	CLK high time	0.4*Tcycle	0.6*Tcycle	At 2 V
Tlow	CLK low time	0.4*Tcycle	0.6*Tcycle	At 0.8 V
Tr/Tf	CLK slew rate[1]	1 V/ns	4 V/ns	–

[1]Rise and fall times are specified in terms of the edge rate measured in V/ns. Parameter design guarantee.

3.4.4 Other PCI Signals

Figure 5 shows the timing diagram characteristics, and Table 15 lists the other PCI signals.

Figure 5 Timing Diagram for Other PCI Signals

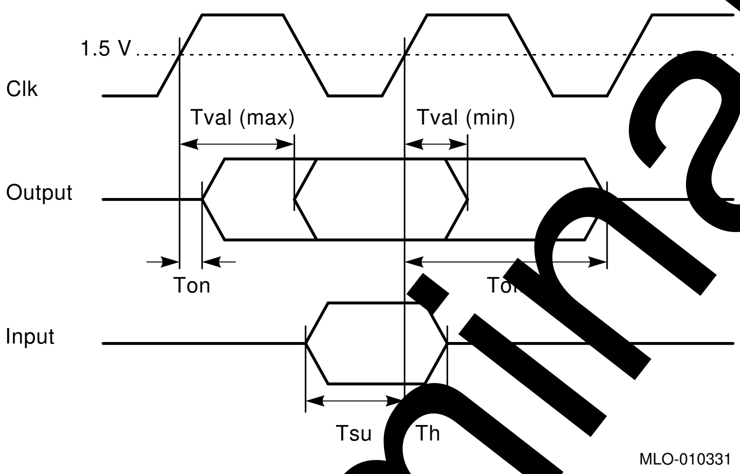


Table 15 Other PCI Signals

Symbol	Parameter	Minimum	Maximum	Conditions
Tval	CLK-to-signal valid delay	2 ns	11 ns	Cload = 50 pF
Ton[1]	Float-to-active delay from CLK	2 ns	–	–
Toff[1]	Active-to-float delay from CLK	Tval (minimum)	28 ns	–
Tsu	Input signal valid setup time before CLK	7 ns	–	–
Th	Input signal hold time from CLK	0 ns	–	–
Tr[1]	Unloaded output rise time	–	2 ns	0.4 V to 2.4 V
Tf[1]	Unloaded output fall time	–	2 ns	2.4 V to 0.4 V

[1]Parameter design guarantee.

3.5 Serial Interface Attachment DC Specifications

Table 16 lists the dc specifications for the external SIA, AUI, and twisted-pair parts of the SIA.

Table 16 SIA DC Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
External SIA Interface Pins					
V_{oh}	Output high voltage	I_{oh} = –4mA	2.4	–	V
V_{ol}	Output low voltage	I_{ol} = 4mA	–	0.4	V
V_{ih}	Input high voltage	–	2.0	–	V
V_{il}	Input low voltage	–	–	0.8	V
I_{oz}	Maximum tristate output leakage current	V_{out} = V_{dd} or V_{ss}	–10	10	μA
AUI Pins					
V_{od}	Transmit differential output voltage (AUI_TD±)	78Ω termination	±550	±1200	mV
V_{odi}[1]	Transmit differential output idle voltage (AUI_TD±)	78Ω termination	–40	+40	mV
I_{odi}[1]	Transmit differential output idle current (AUI_TD±)	78Ω termination	–1	+1	mA

[1]Parameter design guarantee.

(continued on next page)

Table 16 (Cont.) SIA DC Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
AUI Pins					
V_{asq+}[1]	Differential positive squelch threshold (AUI_RD±)	–	175	275	mV
V_{asq-}[1]	Differential negative squelch threshold (AUI_RD± and AUI_CD±)	–	–275	–175	mV
V_{odu}[1]	Transmit differential output undershoot voltage on return to zero (AUI_TD±)	78 Ω termination	–	–100	mV
Twisted-Pair Interface Pins					
V_{toh}	Output high voltage (TP_TD± and TP_TD±±)	I_{oh} = –25 mA	V_{dd} –0.2	V_{dd}	V
V_{tol}	Output low voltage (TP_TD± and TP_TD±±)	I_{ol} = 25 mA	V_{ss}	V_{ss} + 0.2	V
V_{tsq+}[1]	Differential positive squelch threshold (TP_RD±)	–	300	520	mV
V_{tsq-}[1]	Differential negative squelch threshold (TP_RD±)	–	–520	–300	mV
V_{tdif}[1]	Differential input voltage range (TP_RD±)	–	–3.1	3.1	V

[1]Parameter design guarantee.

3.6 Serial Interface Attachment Timing

This section describes the SIA timing limits.

3.6.1 External SIA Mode Timing—Transmit

Figure 6 shows the external SIA transmit timing characteristics, and Table 17 lists the external SIA transmit timing limits.

Figure 6 External SIA Mode Timing Diagram—Transmit

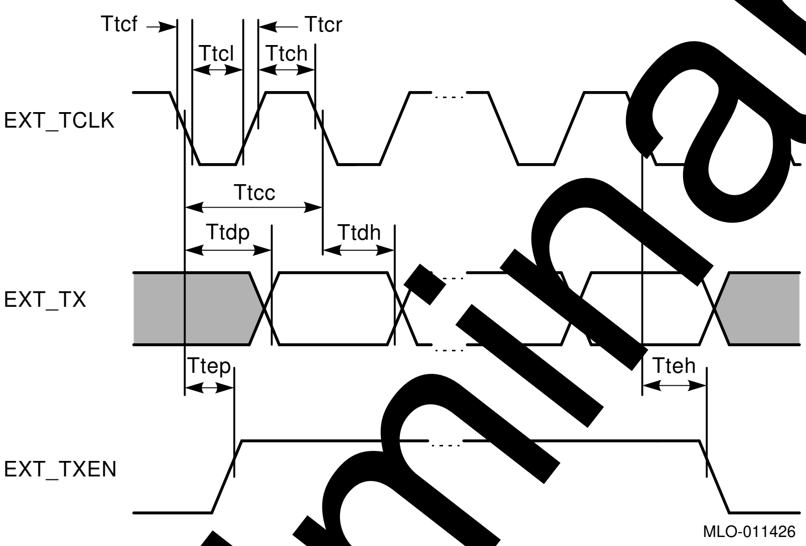


Table 17 External SIA Mode Timing—Transmit

Symbol	Definition	Minimum	Maximum	Units
Ttcc	EXT_TCLK cycle time	99	101	ns
Ttcl	EXT_TCLK low time	45	55	ns
Ttch	EXT_TCLK high time	45	55	ns
Ttcr[1]	EXT_TCLK rise time	–	4	ns
Ttcf[1]	EXT_TCLK fall time	–	4	ns
Ttdp	EXT_TCLK rise to EXT_TX valid	–	40	ns
Ttdh	EXT_TX hold after EXT_TCLK rise	5	–	ns
Ttep	EXT_TCLK rise to EXT_TXEN valid	–	40	ns
Tteh	EXT_TXEN hold after EXT_TCLK fall	5	–	ns

[1]Parameter design guarantee.

3.6.2 External SIA Mode Timing—Collision

Figure 7 shows the external SIA collision timing characteristics, and Table 18 lists external SIA collision timing limits.

Figure 7 External SIA Mode Timing Diagram—Collision

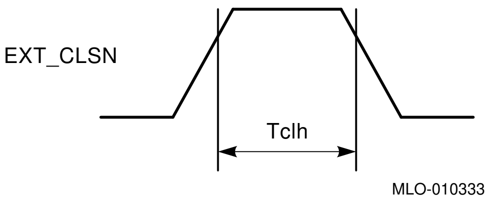


Table 18 External SIA Mode Timing—Collision

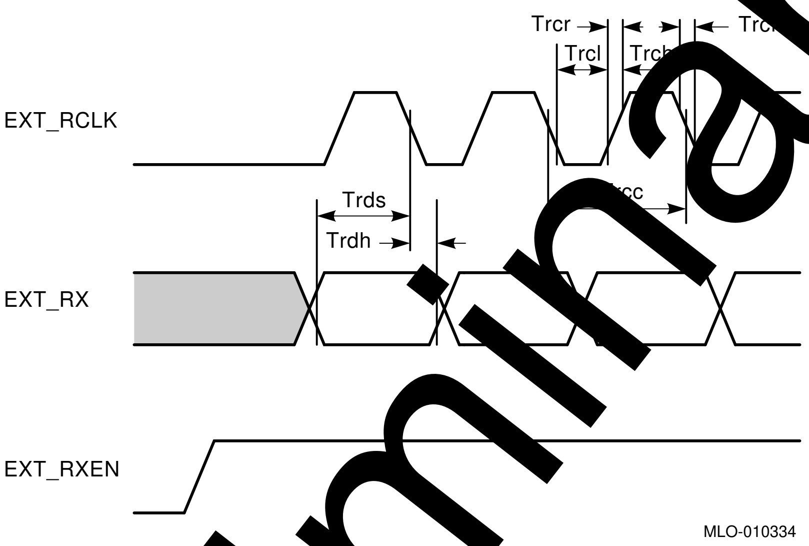
Symbol	Definition	Minimum	Maximum	Units
Tclh[1]	EXT_CLSN high time	40	–	ns

[1]Parameter design guarantee.

3.6.3 External SIA Mode Timing—Receive, Start of Packet

Figure 8 shows the external SIA timing characteristics in receive mode, start of packet.

Figure 8 External SIA Mode Timing Diagram—Receive, Start of Packet



3.6.4 External SIA Mode Timing—Receive, End of Packet

Figure 9 shows the external SIA timing characteristics in receive mode, end of packet; and Table 19 lists the external SIA timing limits in receive mode, end of packet.

Figure 9 External SIA Mode Timing Diagram—Receive, End of Packet

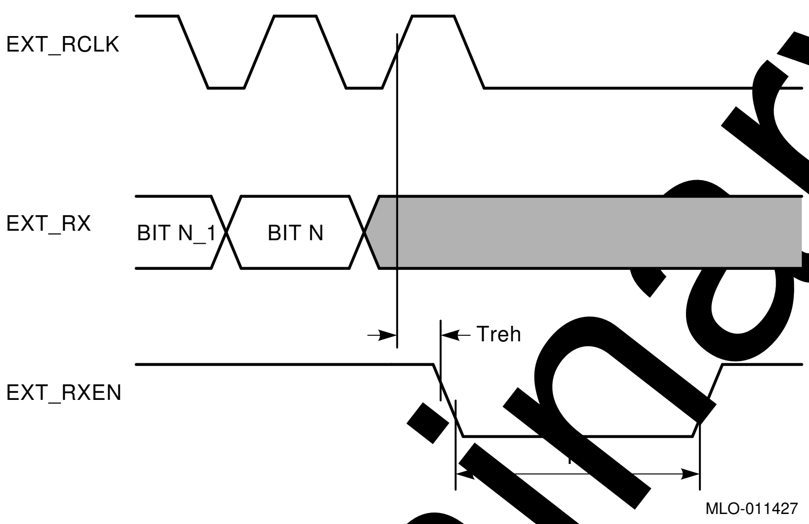


Table 19 External SIA Mode Timing—Receive, Start and End of Packet

Symbol	Definition	Minimum	Maximum	Units
Trcc	EXT_RCLK cycle time	90	118	ns
Trcl	EXT_RCLK low time	38	–	ns
Trch	EXT_RCLK high time	38	–	ns
Trcr[1]	EXT_RCLK rise time	–	4	ns
Trcf[1]	EXT_RCLK fall time	–	4	ns
Trds	EXT_RX setup to EXT_RCLK fall	10	–	ns
Trdh	EXT_RX hold after EXT_RCLK fall	5	–	ns
Treh	EXT_RXEN hold after EXT_RCLK rise	40	–	ns
Trel	EXT_RXEN low time	120	–	ns

[1]Parameter design guarantee.

3.6.5 Internal SIA Mode AUI Timing—Transmit

Figure 10 shows the internal SIA transmit timing characteristics for the AUI, and Table 20 lists the internal SIA transmit timing limits for the AUI.

Figure 10 Internal SIA Mode AUI Timing Diagram—Transmit

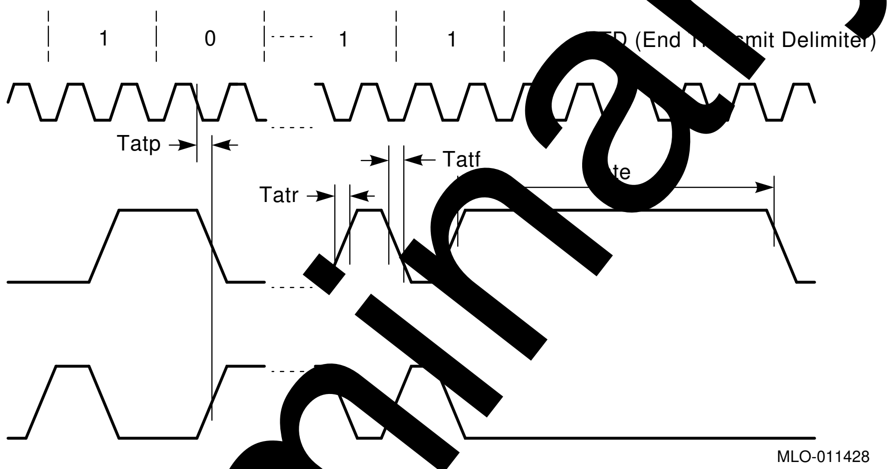


Table 20 Internal SIA Mode AUI Timing—Transmit

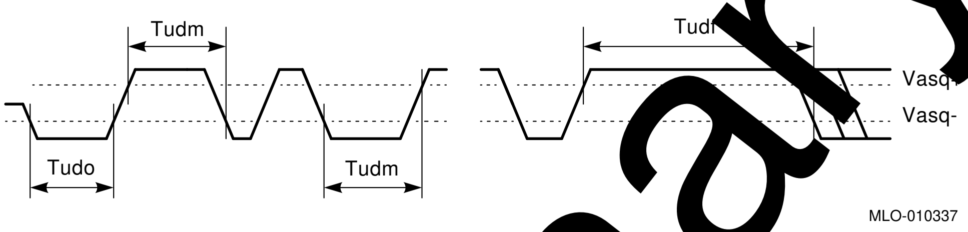
Symbol	Definition	Minimum	Maximum	Units
Tatp	AUI_TD+, AUI_TD– propagation delay from XTAL1 fall	–	30	ns
Tatr[1]	AUI_TD+, AUI_TD– rise time	2	8	ns
Tatf[1]	AUI_TD+, AUI_TD– fall time	2	8	ns
Tatm[1]	AUI_TD+, AUI_TD– rise and fall time mismatch (not shown)	–	1	ns
Tate	AUI_TD+/– end transmit delimiter length	345	405	ns

[1]Parameter design guarantee.

3.6.6 Internal SIA Mode AUI Timing—Receive

Figure 11 shows the internal SIA receive timing characteristics for the AUI.

Figure 11 Internal SIA Mode AUI Timing Diagram—Receive



3.6.7 Internal SIA Mode AUI Timing—Collision

Figure 12 shows the internal SIA collision timing characteristics for the AUI, and Table 21 lists the internal SIA collision timing limits for the AUI.

Figure 12 Internal SIA Mode AUI Timing Diagram—Collision

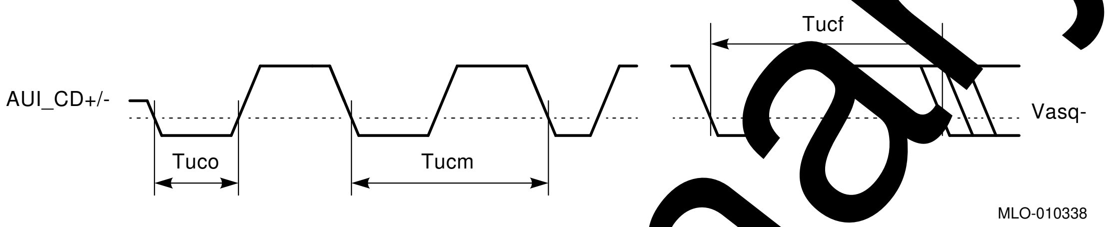


Table 21 Internal SIA Mode AUI Timing—Receive and Collision

Symbol	Definition	Minimum	Maximum	Units
Tudo	AUI_RD+/– start of frame pulse width	20	25	ns
Tudm	AUI_RD+/– delay between opposite squelch crossings not recognized as end of packet	–	140	ns
Tudf	AUI_RD+/– delay from last squelch crossing recognized as end of packet	150	–	ns
Tuco	AUI_CD+/– start of collision pulse width	20	25	ns
Tucm	AUI_CD+/– delay between squelch crossings not recognized as end of collision	–	140	ns
Tucf	AUI_CD+/– delay from last squelch crossing recognized as end of collision	150	–	ns

3.6.8 Internal SIA Mode 10BASE-T Interface Timing—Transmit

Figure 13 shows the internal SIA transmit timing characteristics for the 10BASE-T interface, and Table 22 lists the internal SIA transmit limits.

Figure 13 Internal SIA Mode 10BASE-T Interface Timing Diagram— Transmit

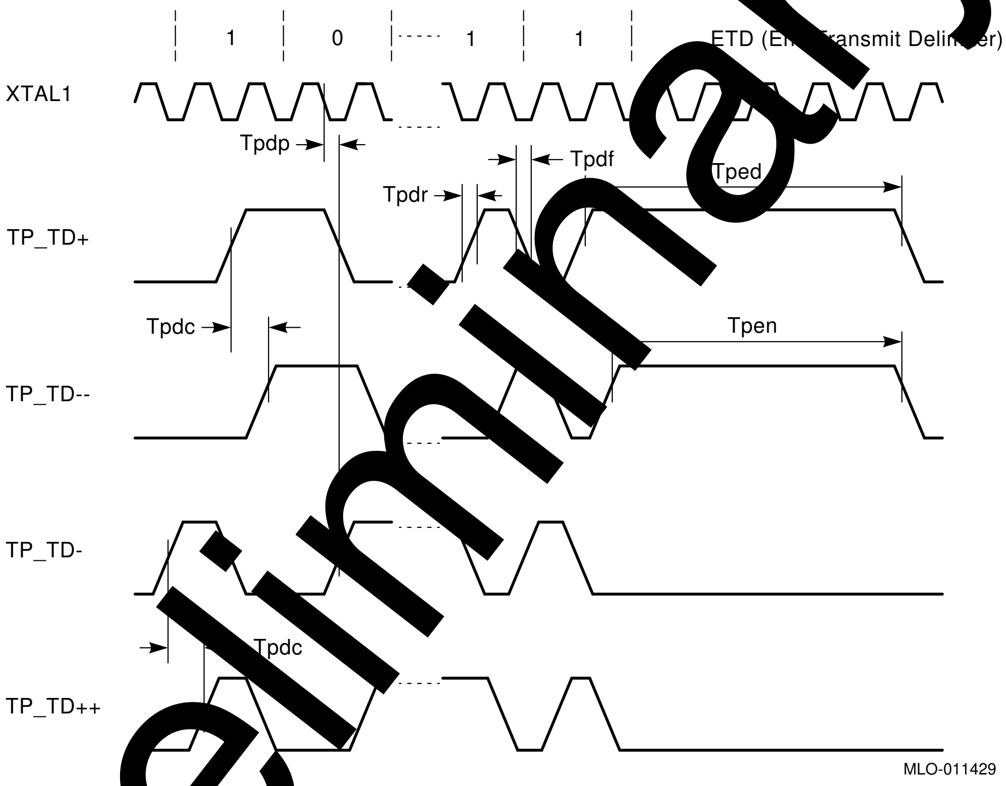


Table 22 Internal SIA Mode 10BASE-T Interface Timing—Transmit

Symbol	Definition	Minimum	Maximum	Units
Tpdp	TP_TD+, TP_TD– propagation delay from XTAL1 fall	–	30	ns
Tpdr[1]	TP_TD+, TP_TD++, TP_TD–, TP_TD– – rise time	2	8	ns
Tpdf[1]	TP_TD+, TP_TD++, TP_TD–, TP_TD– – fall time	2	8	ns
Tpdm[1]	TP_TD+, TP_TD++, TP_TD–, TP_TD– – rise and fall time mismatch (not shown)	–	1	ns
Tpdc	TP_TD+ to TP_TD– – and TP_TD– to TP_TD++ delay	46	54	ns
Tped	TP_TD+/– end transmit delimiter length	295	355	ns
Tpen	TP_TD++/– – end transmit delimiter length	245	305	ns

[1]Parameter design guarantee.

3.6.9 Internal SIA Mode 10BASE-T Interface Timing—Receive

Figure 14 shows the internal SIA receive timing characteristics for the 10BASE-T interface, and Table 23 lists the internal SIA receive limits for the 10BASE-T interface.

Figure 14 Internal SIA Mode 10BASE-T Interface Timing Diagram—Receive

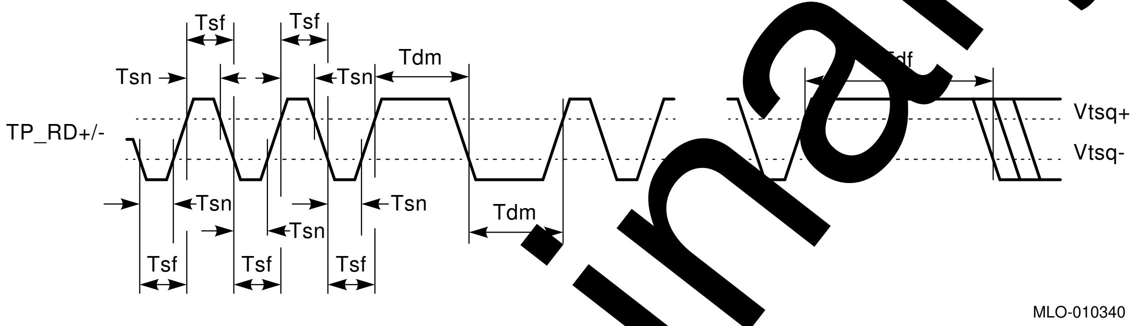


Table 23 Internal SIA Mode 10BASE-T Interface Timing—Receive

Symbol	Definition	Minimum	Maximum	Units
Tsn	TP_RD+/– start of frame pulse width during smart squelch operation	15	20	ns
Tsf	TP_RD+/– maximum delay between opposite squelch crossings to not turn smart squelch off	140	150	ns
Tdm	TP_RD+/– delay between opposite squelch crossings not recognized as end of packet	–	140	ns
Tdf	TP_RD+/– delay from last squelch crossing recognized as end of packet	150	–	ns

3.6.10 Internal SIA Mode 10BASE-T Interface Timing—Idle Link Pulse

Figure 15 shows the internal SIA idle link pulse timing characteristics for the 10BASE-T interface, and Table 24 lists the internal SIA idle link pulse limits for the 10BASE-T interface.

Figure 15 Internal SIA Mode 10BASE-T Interface Timing Diagram—Idle Link Pulse

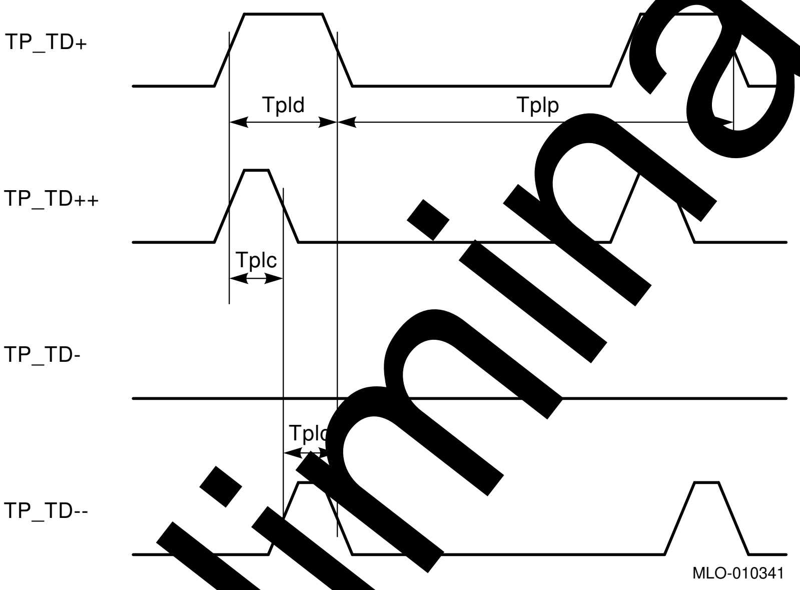


Table 24 Internal SIA Mode 10BASE-T Interface Timing—Idle Link Pulse

Symbol	Definition	Minimum	Maximum	Units
Tpld	TP_TD+ idle link pulse width	80	120	ns
Tplc	TP_TD++ and TP_TD– – idle link pulse width	40	60	ns
Tplp	Idle link pulse period	8	24	ms

3.7 Ethernet ID Port Timing

Figure 16 shows the Ethernet ID port timing, and Table 25 lists the Ethernet ID port limits.

Figure 16 Ethernet ID Port Timing Diagram

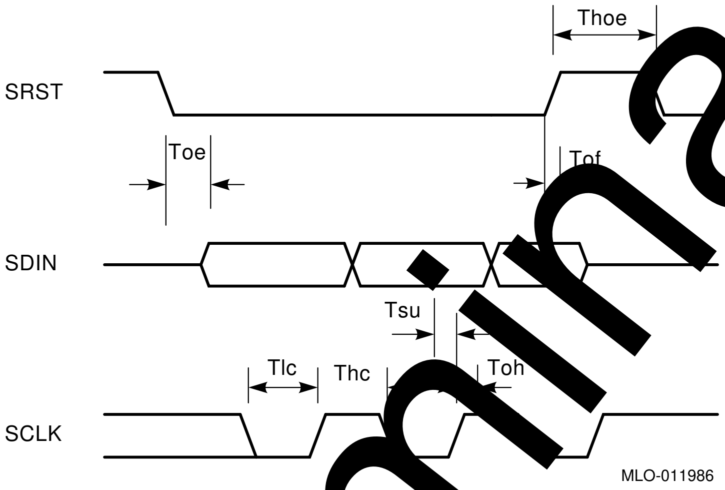


Table 25 Ethernet ID Port Timing Characteristics

Symbol	Definition	Minimum	Maximum	Units
Tlc	SCLK low time	4*Tcycle[1]	4*Tcycle[1]	ns
Thc	SCLK high time	4*Tcycle[1]	4*Tcycle[1]	ns
Toh	SDIN hold from SCLK	0	–	ns
Tsu	SDIN setup time from SCLK	Tcycle[1]	–	ns
Tof[2]	SRST to SDIN float delay	0	–	ns
Thoe	SRST high time	4*Tcycle[1]	–	ns
Toe	SRST to SDIN valid	–	3*Tcycle[1]	ns

[1]Refer to Table 14 for PCI clock specifications.

[2]Parameter design guarantee.

3.8 JTAG Boundary Scan Timing

Figure 17 shows the JTAG boundary scan timing, and Table 26 lists the interface signal timing relationships.

Figure 17 JTAG Boundary Scan Timing Diagram

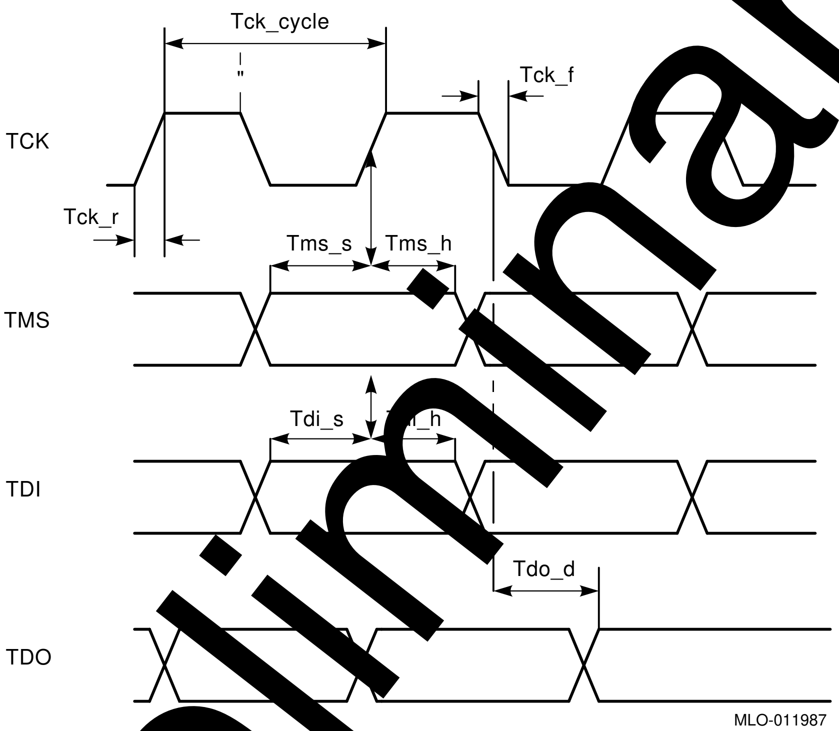


Table 26 JTAG Interface Signal Timing Relationships

Symbol	Parameter	Minimum	Maximum	Units
Tms_s	TMS setup time	20	–	ns
Tms_h	TMS hold time	5	–	ns
Tdi_s	TDI setup time	20	–	ns
Tdi_h	TDI hold time	5	–	ns
Tdo_d	TDO delay time	–	20	ns
Tck_r[1]	TCK rise time	–	3	ns
Tck_f[1]	TCK fall time	–	3	ns
Tck_cycle	TCK cycle time	90	–	ns

[1]Parameter design guarantee.

4 Mechanical Specifications

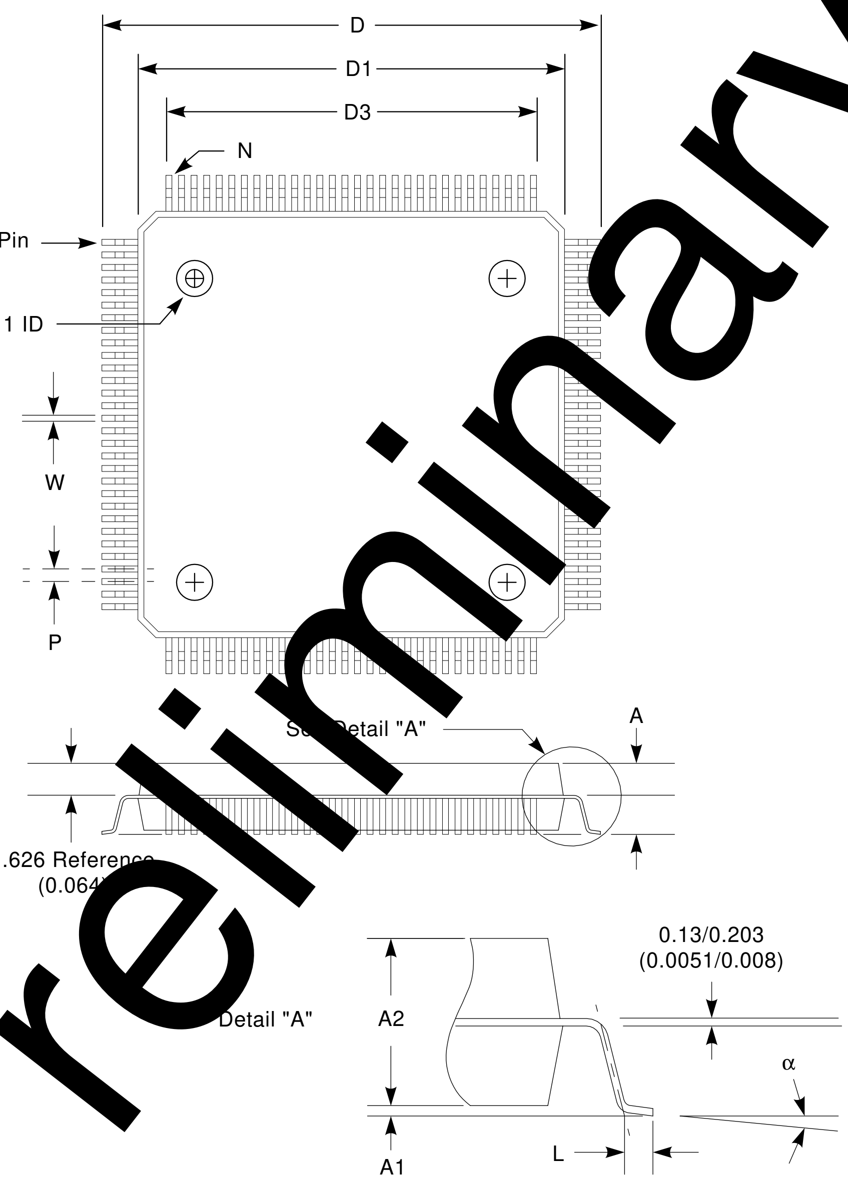
The 21040 is contained in a 120-pin plastic quad flat pack (PQFP). Table 27 lists the mechanical specifications, and Figure 18 shows the mechanical layout of the 21040.

Table 27 Mechanical Features

Item	Minimum[1]	Nominal[1]	Maximum[1]
A	–	–	4.07
A1	0.05	–	–
A2	3.17	3.37	3.67
D	30.90	31.20	31.50
D1	27.80	28.00	28.20
D3	23.20 Reference	23.20 Reference	23.20 Reference
L	0.65	0.80	0.95
N	–	120	–
P	0.80 BSC	0.80 BSC	0.80 BSC
W	0.30	0.35	0.45
α	0°	–	7°

[1]All dimensions are in millimeters.

Figure 18 Mechanical Layout of the DECchip 21040



Note: All dimensions are in millimeters.

MLO-012204

Technical Support, Ordering, and Associated Literature

This section describes how to obtain DECchip information and technical support, as well as how to order DECchip products and associated literature.

Calling the DECchip Information Line for Information and Technical Support

Call the DECchip Information Line for information and technical support:

United States and Canada	**1–800–332–2717 (1–800–DEC–2717)**
TTY (United States only)	**1–800–332–2515 (1–800–DEC–2515)**
Outside North America	**+1–508–568–6868**

Ordering DECchip Products

To order the DECchip 21040 Ethernet LAN Controller for PCI or the DECchip 21040 Evaluation Board Kit, contact your local Digital sales office. When working with your sales representative, you may be able to take advantage of discounts and volume pricing.

You can order the following DECchip products from Digital.

Product	Order Number
DECchip 21040 Ethernet LAN Controller for PCI	21040–AA
DECchip 21040 Evaluation Board Kit	21A40–01

Ordering Associated DECchip Literature

The following table lists some of the DECchip literature that is available. For a complete list, and for information about ordering, contact the DECchip Information Line.

Title	Order Number
Alpha Architecture Reference Manual[1]	EY–L520E–DP–YCH
DECchip 21040 Ethernet LAN Controller for PCI Product Brief	EC–N0281–72
DECchip 21040 Ethernet LAN Controller for PCI Data Sheet	EC–N0280–72
DECchip 21040 Ethernet LAN Controller for PCI Hardware Reference Manual	EC–N0752–72
DECchip 21040 PCI Evaluation Board User's Guide	EC–N0753–72
Connecting the DECchip Ethernet LAN Controller to the Network: An Application Note	EC–N0737–72
Ethernet Address ROM Programming: An Application Note	EC–N3214-72

[1]To order and purchase the *Alpha Architecture Reference Manual*, call **1–800–DIGITAL** from the U.S. or Canada, or contact your local Digital office, or technical or reference bookstore where Digital Press books are distributed by Prentice Hall.